**Sri Krishnadevaraya University College of Engineering & Technology**
**Ananthapuramu-515003(A.P) India**
**Electronics and Communication Engineering**

## Draft Academic Regulations of M.Tech. (Full Time/Regular) Programme
**(Effective for the students admitted into M.Tech. I year from the Academic Year 2024-25 onwards)**

Sri Krishnadevaraya University College of Engineering & Technology offers **Two** Years (**Four** Semesters) full-time Master of Technology (M.Tech.) Degree programme, under Choice Based Credit System (CBCS) in different branches of Engineering and Technology with different specializations.
Sri Krishnadevaraya University College of Engineering & Technology, Ananthapuramu shall confer M. Tech. degree on candidates who are admitted to the programme and fulfill all the requirements for the award of the degree.

1. **Award of the M.Tech. Degree**
   A student will be declared eligible for the award of the M.Tech. degree if he/she fulfils the following:
   1.1 Pursues a course of study for not less than two academic years and not more than four academic years.
   1.2 Registers for 70 credits and secures all 70 credits.

2. Students, who fail to fulfil all the academic requirements for the award of the degree within four academic years from the year of their admission, shall forfeit their seat in M.Tech. course and their admission stands cancelled.

3. **Programme of Study:**
   The following M.Tech. Specializations are offered at present in different branches of Engineering and Technology:

| S.No. | Branch | Name of the Specialization |
|---|---|---|
| 01 | Computer Science and Engineering | Computer Science and Engineering |
| 02 | Electronics and Communication Engineering | Embedded Systems & VLSI Design |
| 03 | Electrical and Electronics Engineering | Electrical Power Systems |

4. **Eligibility for Admissions**:
   4.1 Admission to the M. Tech Program shall be made subject to the eligibility, qualification and specialization prescribed by the A.P. State Government/University from time to time.
   4.2 Admissions shall be made either on the basis of the merit rank or Percentile obtained by the qualified student in the relevant qualifying GATE Examination/ the merit rank obtained by the qualified student in an entrance test conducted by A.P. State Government (APPGECET) for M.Tech. programmes/an entrance test conducted by University/on the basis of any other exams approved by the University, subject to reservations as laid down by the Govt. from time to time.

5. **Programme related terms:**
   5.1 ***Credit:*** A unit by which the course work is measured. It determines the number of hours of instructions required per week. One credit is equivalent to one hour of teaching (Lecture/Tutorial) or two hours of practical work/field work per week.
   Credit definition:

| | |
|---|---|
| 1 Hr. Lecture (L) per week | 1 credit |
| 1 Hr. Tutorial (T) per week | 1 credit |

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| | |
|---|---|
| 1 Hr. Practical (P) per week | 0.5 credit |

5.2 ***Academic Year:*** Two consecutive (one odd + one even) semesters constitute one academic year.

5.3 ***Choice Based Credit System (CBCS):*** The CBCS provides choice for students to select from the prescribed courses.

## 6. Programme Pattern:

6.1 Total duration of the of M.Tech. programme is two academic years

6.2 Each academic year of study is divided into two semesters.

6.3 Each Semester shall be of 22 weeks duration (inclusive of Examinations), with a minimum of 90 instructional days per semester.

6.4 The student shall not take more than four academic years to fulfill all the academic requirements for the award of M.Tech. degree from the date of commencement of first year first semester, failing which the student shall forfeit the seat in M.Tech. programme.

6.5 The medium of instruction of the programme (including examinations and project reports) will be in English only.

6.6 All subjects/courses offered for the M.Tech. degree programme are broadly classified as follows:

| S.No. | Broad Course Classification | Course Category | Description |
|---|---|---|---|
| 1. | Core Courses | Foundational & Professional Core Courses (PC) | Includes subjects related to the parent discipline/department/branch of Engineering |
| 2. | Elective Courses | Professional Elective Courses (PE) | Includes elective subjects related to the parent discipline/department/ branch of Engineering |
| | | Open Elective Courses (OE) | Elective subjects which include inter-disciplinary subjects or subjects in an area outside the parent discipline which are of importance in the context of special skill development |
| 3. | Research | Research methodology & IPR | To understand importance and process of creation of patents through research |
| | | Technical Seminar | Ensures preparedness of students to undertake major projects/Dissertation, based on core contents related to specialization |
| | | Cocurricular Activities | Attending conferences, scientific presentations and other scholarly activities |
| | | Dissertation | M.Tech. Project or Major Project |
| 4. | Audit Courses | Mandatory noncredit courses | Covering subjects of developing desired attitude among the learners is on the line of initiatives such as Unnat Bharat Abhiyan, Yoga, Value education etc. |

6.7 The college shall take measures to implement Virtual Labs (https://www.vlab.co.in) which provide remote access to labs in various disciplines of Engineering and will help student in learning basic and advanced concept through remote experimentation. Student shall be made to work on virtual lab experiments during the regular labs.

6.8 A faculty advisor/mentor shall be assigned to each specialization to advise students on the programme, its Course Structure and Curriculum, Choice of Courses, based on his competence, progress, pre-requisites and interest.

6.9 Preferably 25% course work for the theory courses in every semester shall be conducted in the blended mode of learning.

**7. Attendance Requirements:**

7.1 A student shall be eligible to appear for the University external examinations if he/she acquires 75% of attendance in aggregate of all the courses.

7.2 Condonation of shortage of attendance in aggregate up to 10% (65% and above and below 75%) in each semester may be granted by the College Academic Committee.

7.3 Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representation by the candidate with supporting evidence

7.4 Students whose shortage of attendance is not condoned in any semester are not eligible to take their end examination of that class.

7.5 A stipulated fee shall be payable towards condonation of shortage of attendance.

7.6 A student will not be promoted to the next semester unless he satisfies the attendance requirements of the present semester. They may seek re-admission into that semester when offered next.

7.7 If any candidate fulfils the attendance requirement in the present semester, he shall not be eligible for readmission into the same class.

7.8 If the learning is carried out in blended mode (both offline & online), then the total attendance of the student shall be calculated considering the offline and online attendance of the student.

**8. Evaluation – Distribution and Weightage of Marks:**

The performance of a student in each semester shall be evaluated subject - wise (irrespective of credits assigned), for a maximum of 100 marks for theory and 100marks for practical, based on Internal Evaluation and End Semester Examination.

8.1 There shall be five units in each of the theory subjects. For the theory subjects 60 marks will be for the End Examination and 40 marks will be for Internal Evaluation.

8.2 Two Internal Examinations shall be conducted for 30 marks each, one in the middle of the Semester and the other immediately after the completion of instruction. First mid examination shall be conducted for I & II units of the syllabus and second mid examination for III, IV & V units. Each mid exam shall be conducted for a total duration of 120 minutes with 3 questions (without choice) each question for 10 marks. Final Internal marks for a total of 30 marks shall be arrived at by considering the marks secured by the student in both the internal examinations with 80% weightage to the better internal exam and 20% to the other. There shall be two online examinations conducted during the respective mid examinations by the college for the remaining 10 marks with 20 objective questions.

8.3 The following pattern shall be followed in the End Examination:

i. Five questions shall be set from each of the five units with either/or type for 12 marks each.
ii. All the questions have to be answered compulsorily.
iii. Each question may consist of one, two or more bits.

8.4 For practical subjects, 60 marks shall be for the End Semester Examinations and 40 marks will be for internal evaluation based on the day-to-day performance.
The internal evaluation based on the day-to-day work-10 marks, record- 10 marks and the remaining 20 marks to be awarded by conducting an internal laboratory test. The end examination shall be conducted by the examiners, with a breakup mark of Procedure-10, Experimentation-25, Results-10, Viva- voce-15

8.5 There shall be a **Technical Seminar** during I year II semester for internal evaluation of 100 marks. A student under the supervision of a faculty member, shall

collect the literature on a topic and critically review the literature and submit it to the department in a report form and shall make an oral presentation before the Project Review Committee consisting of Head of the Department, supervisor/mentor and two other faculty members of the department. The student must secure a minimum of 50% of marks, to be declared successful. If he fails to obtain the minimum marks, he must reappear for the same as and when supplementary examinations are conducted. The Technical seminar shall be conducted anytime during the semester as per the convenience of the Project Review Committee and students. There shall be no external examination for Technical Seminar.

8.6 There shall be Mandatory **Audit courses** in I & II semesters for zero credits. There is no external examination for audit courses. However, attendance shall be considered while calculating aggregate attendance and student shall be declared to have passed the mandatory course only when he/she secures 50% or more in the internal examinations. In case, the student fails, a re- examination shall be conducted for failed candidates for 40 marks every six months/semester satisfying the conditions mentioned in item 1 & 2 of the regulations.

8.7 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Semester Examination and Internal Evaluation taken together.

8.8 In case the candidate does not secure the minimum academic requirement in any of the subjects he/she has to reappear for the Semester Examination either supplementary or regular in that subject or repeat the course when next offered or do any other specified subject as may be required.

8.9 The laboratory records and mid semester test papers shall be preserved for a minimum of 3 years in the respective institutions as per the University norms.

## 9. Credit Transfer Policy

As per University Grants Commission (Credit Framework for Online Learning Courses through SWAYAM) Regulation, 2016, the University shall allow up to a maximum of 40% of the total courses being offered in a particular Programme in a semester through the Online Learning courses through SWAYAM.

9.1 The University shall offer credit mobility for MOOCs and give the equivalent credit weightage to the students for the credits earned through online learning courses through SWAYAM platform.

9.2 The online learning courses available on the SWAYAM platform will be considered for credit transfer. SWAYAM course credits are as specified in the platform

9.3 Student registration for the MOOCs shall be only through the institution, it is mandatory for the student to share necessary information with the institution

9.4 The institution shall select the courses to be permitted for credit transfer through SWAYAM. However, while selecting courses in the online platform institution would essentially avoid the courses offered through the curriculum in the offline mode.

9.5 The institution shall notify at the beginning of semester the list of the online learning courses eligible for credit transfer in the forthcoming Semester.

9.6 The institution shall also ensure that the student has to complete the course and produce the course completion certificate as per the academic schedule given for the regular courses in that semester

9.7 The institution shall designate a faculty member as a Mentor for each course to guide the students from registration till completion of the credit course.

9.8 The university shall ensure no overlap of SWAYAM MOOC exams with that of the university examination schedule. In case of delay in SWAYAM results, the university will re-issue the marks sheet for such students.

9.9 Student pursuing courses under MOOCs shall acquire the required credits only after successful completion of the course and submitting a certificate issued by the competent authority along with the percentage of marks and grades.

9.10 The institution shall submit the following to the examination section of the university:

a) List of students who have passed MOOC courses in the current semester along with the certificates of completion.

b) Undertaking form filled by the students for credit transfer.

9.11 The university shall resolve any issues that may arise in the implementation of this policy from time to time and shall review its credit transfer policy in the light of periodic changes brought by UGC, SWAYAM, NPTEL and state government.

**Note:** Students shall also be permitted to register for MOOCs offered through online platforms other than SWAYAM NPTEL. In such cases, credit transfer shall be permitted only after seeking approval.

**10. Re-registration for Improvement of Internal Evaluation Marks:**

A candidate shall be given one chance to re-register for each subject provided the internal marks secured by a candidate are less than 50% and has failed in the end examination

10.1 The candidate should have completed the course work and obtained examinations results for I, II and III semesters.

10.2 The candidate should have passed all the subjects for which the Internal Evaluation marks secured are more than 50%.

10.3 Out of the subjects the candidate has failed in the examination due to Internal Evaluation marks secured being less than 50%, the candidate shall be given one chance for each Theory subject and for a maximum of three Theory subjects for Improvement of Internal evaluation marks.

10.4 The candidate has to re-register for the chosen subjects and fulfill the academic requirements.

10.5 For reregistration the candidates have to apply to the University through the college by paying the requisite fees and get approval from the University before the start of the semester in which re-registration is required

10.6 In the event of availing the Improvement of Internal evaluation marks, the internal evaluation marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

**11. Evaluation of Project/Dissertation Work:**

The Project work shall be initiated at the beginning of the III Semester and the duration of the Project is of two semesters. Evaluation of Project work is for 300 marks with 200 marks for internal evaluation and 100 marks for external evaluation. Internal evaluation of the Project Work – I & Project work – II in III & IV semesters respectively shall be for 100 marks each. External evaluation of final Project work viva voce in IV semester shall be for 100 marks.

A Project Review Committee (PRC) shall be constituted with the Head of the Department

as Chairperson, Project Supervisor and one faculty member of the department offering the M.Tech. programme.

11.1 A candidate is permitted to register for the Project Work in III Semester after satisfying the attendance requirement in all the subjects, both theory and laboratory (in I & II semesters).

11.2 A candidate is permitted to submit Project dissertation with the approval of PRC. The candidate has to pass all the theory, practical and other courses before submission of the Thesis.

11.4 Project work shall be carried out under the supervision of teacher in the parent department concerned.

11.5 A candidate shall be permitted to work on the project in an industry/research organization on the recommendation of the Head of the Department. In such cases,one of the teachers from the department concerned would be the internal guide and an expert from the industry/ research organization concerned shall act as co-supervisor/ external guide. It is mandatory for the candidate to make full disclosure of all data/results on which they wish to base their dissertation. They cannot claim confidentiality simply because it would come into conflict with the Industry's or R&D laboratory's own interests. A certificate from the external supervisor is to be included in the dissertation.

11.6 Continuous assessment of Project Work - I and Project Work – II in III & IV semesters respectively will be monitored by the PRC.

11.7 The candidate shall submit status report by giving seminars in three different phases (two in III semester and one in IV semester) during the project work period. These seminar reports must be approved by the PRC before submission of the Project Thesis.

11.8 After registration, a candidate must present in Project Work Review - I, in consultation with his Project Supervisor, the title, objective and plan of action of his Project work to the PRC for approval within four weeks from the commencement of III Semester. Only after obtaining the approval of the PRC can the student initiate the project work.

11.9 The Project Work Review - II in III semester carries internal marks of 100. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate the work for the other 50 marks. The Supervisor and PRC will examine the Problem Definition, Objectives, Scope of Work, Literature Survey in the same domain and progress of the Project Work.

11.10 A candidate has to secure a minimum of 50% of marks to be declared successful in Project Work Review - II. Only after successful completion of Project Work Review – II, candidate shall be permitted for Project Work Review – III in IV Semester. The unsuccessful students in Project Work Review - II shall reappear for it as and when supplementary examinations are conducted.

11.11 The Project Work Review - III in IV semester carries 100 internal marks. Evaluation should be done by the PRC for 50 marks and the Supervisor will evaluate it for the other 50 marks. The PRC will examine the overall progressof the Project Work and decide whether or not eligible for final submission. A candidate has to secure a minimum of 50% of marks to be declared successful in Project Work Review - III. If he fails to obtain the required minimum marks, he has to reappear for Project Work Review - III after a month.

11.12 For the approval of PRC the candidate shall submit the draft copy of dissertation to the Head of the Department and make an oral presentation before the PRC.

11.13 After approval from the PRC, the students are required to submit a report showing that the plagiarism is within 30%. The dissertation report will be accepted only when the plagiarism is within 30%, which shall be submitted along with the dissertation report.

11.14 Research paper related to the Project Work shall be published in conference proceedings/UGC recognized journal. A copy of the published research paper shall be attached to the dissertation.

11.15 After successful plagiarism check and publication of research paper, three copies of the dissertation certified by the supervisor and HOD shall be submitted to the College.

11.16 The dissertation shall be adjudicated by an external examiner selected by the University. For this, the Principal of the College shall submit a panel of three examiners as submitted by the supervisor concerned and department head for each student. However, the dissertation will be adjudicated by one examiner nominated by the University.

11.17 If the report of the examiner is not satisfactory, the candidate shall revise and resubmit the dissertation, in the time frame as decided by the PRC. If report of the examiner is unfavorable again, the thesis shall be summarily rejected. The candidate has to reregister for the project and complete the project within the stipulated time after taking the approval from the University

11.18 If the report of the examiner is satisfactory, the Head of the Department shall coordinate and make arrangements for the conduct of Project Viva voce exam.

11.19 The Project Viva voce examinations shall be conducted by a board consisting of the Supervisor, Head of the Department and the external examiner who has adjudicated the dissertation. For Dissertation Evaluation (Viva voce) in IV Sem. there are external marks of 100 and it is evaluated by external examiner. The candidate must secure a minimum of 50% marks in Viva voce exam.

11.20 If he fails to fulfill the requirements as specified, he will reappear for the Project Viva voce examination only after three months. In the reappeared examination also, if he fails to fulfill the requirements, he will not be eligible for the award of the degree.

## 12. Credits for Co-curricular Activities

The credits assigned for co-curricular activities shall be given by the principals of the colleges and the same shall be submitted to the University.

A Student shall earn 02 credits under the head of co-curricular activities, viz., attending Conference, Scientific Presentations and Other Scholarly Activities.

Following are the guidelines for awarding Credits for Co-curricular Activities

| Name of the Activity | Maximum Credits / Activity |
|---|---|
| Participation in National Level Seminar/ Conference / Workshop /Training programs (related to the specialization of the student) | 1 |
| Participation in International Level Seminar / Conference / workshop/Training programs held outside India (related to the specialization of the student) | 2 |
| Academic Award/Research Award from State Level/National Agencies | 1 |
| Academic Award/Research Award from International Agencies | 2 |
| Research / Review Publication in National Journals (Indexed in Scopus / Web of Science) | 1 |

| | |
|---|---|
| Research / Review Publication in International Journals with Editorial board outside India (Indexed in Scopus / Web of Science) | 2 |

**Note:**

i) Credit shall be awarded only for the first author. Certificate of attendance and participation in a Conference/Seminar is to be submitted for awarding credit.

ii) Certificate of attendance and participation in workshops and training programs (Internal or External) is to be submitted for awarding credit. The total duration should be at least one week.

iii) Participation in any activity shall be permitted only once for acquiring required credits under cocurricular activities

## 13. Grading:

As a measure of the student's performance, a 10-point Absolute Grading System using the following Letter Grades and corresponding percentage of marks shall be followed:

After each course is evaluated for 100 marks, the marks obtained in each course will be converted to a corresponding letter grade as given below, depending on the range in which the marks obtained by the student fall.

**Structure of Grading of Academic Performance**

| Range in which the marks in the subject fall | Grade | Grade points Assigned |
|---|---|---|
| ≥ 90 | S (Superior) | 10 |
| ≥ 80 & < 90 | A (Excellent) | 9 |
| ≥ 70 & < 80 | B (Very Good) | 8 |
| ≥ 60 & < 70 | C (Good) | 7 |
| ≥ 50 & < 60 | D (Pass) | 6 |
| < 50 | F (Fail) | 0 |
| Absent | Ab (Absent) | 0 |

A student obtaining Grade 'F' or Grade 'Ab' in a subject shall be considered failed and will be required to reappear for that subject when it is offered in the next supplementary examination.

i) For noncredit audit courses, "Satisfactory" or "Unsatisfactory" shall be indicated instead of the letter grade and this will not be counted for the computation of SGPA/CGPA/Percentage.

**Computation of Semester Grade Point Average (SGPA) and Cumulative Grade Point Average (CGPA):**

The Semester Grade Point Average (SGPA) is the ratio of sum of the product of the number of credits with the grade points scored by a student in all the courses taken by a student and the sum of the number of credits of all the courses undergone by a student, i.e.,

$$SGPA = \Sigma (C_i \times G_i)/\Sigma C_i$$

where, $C_i$ is the number of credits of the $i^{th}$ subject and $G_i$ is the grade point scored by the student in the $i^{th}$ course.

i) The Cumulative Grade Point Average (CGPA) will be computed in the same manner considering all the courses undergone by a student over all the semesters of a program, i.e.,

$$CGPA = \Sigma (C_i \times S_i) / \Sigma C_i$$

where "$S_i$" is the SGPA of the $i^{th}$ semester and $C_i$ is the total number of credits of $i^{th}$ semester.

ii) Both SGPA and CGPA shall be rounded off to 2 decimal points and reported in the transcripts.

iii) While computing the SGPA the subjects in which the student is awarded Zero grade points will also be included.

Grade Point: It is a numerical weight allotted to each letter grade on a 10-point scale. Letter Grade: It is an index of the performance of students in a said course. Grades are denoted by letters S, A, B, C, D and F.

**14. Award of Class:**

After a student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree, he shall be placed in one of the following three classes:

| Class Awarded | Percentage of Marks to be secured |
|---|---|
| First Class with Distinction | ≥70% |
| First Class | < 70% ≥ 60% |
| Pass Class | < 60% ≥ 50% |

**15. Exit Policy:** The student shall be permitted to exit with a PG Diploma based on his/her request to the university through the institution at the end of first year subject to passing all the courses in first year.

The University shall resolve any issues that may arise in the implementation of this policy from time to time and shall review the policy in the light of periodic changes brought by UGC, AICTE and State government.

**16. Withholding of Results:**

If the candidate has any case of in-discipline pending against him, the result of the candidate shall be withheld, and he will not be allowed/promoted into the next higher semester. The issue of degree is liable to be withheld in such cases.

**17. Transitory Regulations**

Discontinued, detained, or failed candidates are eligible for readmission as and when the semester is offered after fulfilment of academic regulations. Candidates who have been detained for want of attendance or not fulfilled academic requirements or who have failed after having undergone the course in earlier regulations or have discontinued and wish to continue the course are eligible for admission into the unfinished semester from the date of commencement of class work with the same or equivalent subjects as and when subjects are offered, subject to Section 2 and they will follow the academic regulations into which they are readmitted.

**18. General:**

18.1 The academic regulations should be read for purpose of any interpretation.

18.2 Disciplinary action for Malpractice/improper conduct in examinations is appended.

18.3 Where the words "he", "him", "his", occur in the regulations, they include "she",

"her", "hers".

18.4 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the Vice-Chancellor is final.

18.5 The University may change or amend the academic regulations or syllabi at any time and the changes or amendments shall be made applicable to all the students on rolls with effect from the dates notified by the University.

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# RULES FOR

## DISCIPLINARY ACTION FOR MALPRACTICES / IMPROPER CONDUCT IN EXAMINATIONS

| | Nature of Malpractices/Improper conduct | Punishment |
|---|---|---|
| | *If the candidate:* | |
| 1.(a) | Possesses or keeps accessible in examination hall, any paper, note book, programmable calculators, Cell phones, pager, palm computers or any other form of material concerned with or related to the subject of the examination (theory or practical) in which he is appearing but has not made use of (material shall include any marks on the body of the candidate which can be used as an aid in the subject of the examination) | Expulsion from the examination hall and cancellation of the performance in that subject only. |
| (b) | Gives assistance or guidance or receives it from any other candidate orally or by any other body language methods or communicates through cell phones with any candidate or persons in or outside the exam hall in respect of any matter. | Expulsion from the examination hall and cancellation of the performance in that subject only of all the candidates involved. In case of an outsider, he will be handed over to the police and a case is registered against him. |
| 2. | Has copied in the examination hall from any paper, book, programmable calculators, palm computers or any other form of material relevant to the subject of the examination (theory or practical) in which the candidate is appearing. | Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. The Hall Ticket of the candidate is to be cancelled and sent to the University. |
| 3. | Impersonates any other candidate in connection with the examination. | The candidate who has impersonated shall be expelled from examination hall. The candidate is also debarred for four consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. The performance of the original candidate who has been impersonated, shall be cancelled in all the subjects of the examination (including practicals and project work) already appeared and shall not be allowed to appear for examinations of the remaining subjects of that semester/year. The candidate is also debarred for four consecutive semesters from class work and all University examinations if his involvement is established. Otherwise, the candidate is debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. If the imposter is an outsider, he will be handed over to the police and a case is registered against him. |

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| 4. | Smuggles in the Answer book or additional sheet or takes out or arranges to send out the question paper during the examination or answer book or additional sheet, during or after the examination. | Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. |
| 5. | Uses objectionable, abusive or offensive language in the answer paper or in letters to the examiners or writes to the examiner requesting him to award pass marks. | Cancellation of the performance in that subject only. |
| 6. | Refuses to obey the orders of the Chief Superintendent /Assistant - Superintendent /any officer on duty or misbehaves or creates disturbance of any kind in and around the examination hall or organizes a walk out or instigates others to walk out, or threatens the officer-in charge or any person on duty in or outside the examination hall of any injury to his person or to any of his relations whether by words, either spoken or written or by signs or by visible representation, assaults the officer-in-charge, or any person on duty in or outside the examination hall or any of his relations, or indulges in any other act of misconduct or mischief which result in damage to or destruction of property in the examination hall or any part of the College campus or engages in any other act which in the opinion of the officer on duty amounts to use of unfair means or misconduct or has the tendency to disrupt the orderly conduct of the examination. | In case of students of the college, they shall be expelled from examination halls and cancellation of their performance in that subject and all other subjects the candidate(s) has (have) already appeared and shall not be permitted to appear for the remaining examinations of the subjects of that semester/year. If the candidate physically assaults the invigilator/ officer-in-charge of the Examinations, then the candidate is also debarred and forfeits his/her seat. In case of outsiders, they will be handed over to the police and a police case is registered against them. |
| 7. | Leaves the exam hall taking away answer script or intentionally tears of the script or any part thereof inside or outside the examination hall. | Expulsion from the examination hall and cancellation of performance in that subject and all the other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred for two consecutive semesters from class work and all University examinations. The continuation of the course by the candidate is subject to the academic regulations in connection with forfeiture of seat. |
| 8. | Possess any lethal weapon or firearm in the examination hall. | Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. |
| 9. | If student of the college, who is not a candidate for the particular examination or any person not connected with the college indulges in any malpractice or improper conduct mentioned in clause 6 to 8. | Student of the colleges expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project |

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| | | work and shall not be permitted for the remaining examinations of the subjects of that semester/year. The candidate is also debarred and forfeits the seat. Person (s) who do not belong to the College will be handed over to police and, a police case will be registered against them. |
| 10. | Comes in a drunken condition to the examination hall. | Expulsion from the examination hall and cancellation of the performance in that subject and all other subjects the candidate has already appeared including practical examinations and project work and shall not be permitted for the remaining examinations of the subjects of that semester/year. |
| 11. | Copying detected on the basis of internal evidence, such as, during valuation or during special scrutiny. | Cancellation of the performance in that subject only or in that subject and all other subjects the candidate has appeared including practical examinations and project work of that semester / year examinations, depending on the recommendation of the committee. |
| 12. | If any malpractice is detected which is not covered in the above clauses 1 to 11 shall be reported to the University for further action to award suitable punishment. | |

1. Malpractices identified by squad or special invigilators
2. Punishments to the candidates as per the above guidelines.
3. Punishment for institutions: (if the squad reports that the college is also involved in encouraging malpractices)
4. A show cause notice shall be issued to the college.
5. Impose a suitable fine on the college.
6. Shifting the examination center from the college to another college for a specific period of not less than one year.

**Note:**

Whenever the performance of a student is cancelled in any subject/subjects due to Malpractice, he has to register for End Examinations in that subject/subjects consequently and has to fulfil all the norms required for the award of Degree.

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**Sri Krishnadevaraya University College of Engineering & Technology**
**Ananthapuramu-515003(A.P) India**
**Electronics and Communication Engineering**

| **SKUCET Curriculum** |
|---|
| **M.Tech Course Structure – R24** |
| **EMBEDDED SYSTEMS & VLSI DESIGN (EMVL)** |

| **Semester – I** | | | | | |
|---|---|---|---|---|---|
| **Embedded Systems & VLSI Design (EMVL)** | | | | | |
| **S.No** | **Course Code** | **Course Name** | **Category** | **L-T-P** | **Credits** |
| 1 | | Microcontroller Architecture and Organization | PC | 3-0-0 | 3 |
| 2 | | CMOS Digital IC Design | PC | 3-0-0 | 3 |
| 3 | | **Program Elective-I**<br>Communication Buses and Interfaces<br>Data Acquisition System Design<br>FPGA Architectures and Applications<br>Memory Technologies | PE | 3-0-0 | 3 |
| 4 | | **Program Elective-II**<br>Low Power VLSI Design<br>Nanomaterials and Nanotechnology<br>Network Security and Cryptography | PE | 3-0-0 | 3 |
| 5 | | Microcontrollers Lab | PC | 0-0-4 | 2 |
| 6 | | CMOS Digital IC Design Lab | PC | 0-0-4 | 2 |
| 7 | | Research Methodology and IPR | MC | 2-0-0 | 2 |
| 8 | | **Audit Course – I**<br>English for Research paper writing Disaster Management<br>Sanskrit for Technical Knowledge | AC | 2-0-0 | 0 |
| **TOTAL** | | | | | **18** |

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|---|---|---|---|---|---|
| **Embedded Systems & VLSI Design (EMVL)** | | | | | |
| **Semester – II** | | | | | |
| **S.No** | **Course Code** | **Course Name** | **Category** | **L-T-P** | **Credits** |
| **1.** | | CMOS Analog IC Design | PC | 3-0-0 | 3 |
| **2.** | | Embedded System Design | PC | 3-0-0 | 3 |
| **3.** | | **Program Elective – III**<br>Pattern Recognition and Machine Learning<br>Programming Languages for Embedded SoftwareRF IC Design | PE | 3-0-0 | 3 |
| **4.** | | **Program Elective – IV**<br>SoC Architecture<br>System Design with Embedded Linux<br>Physical Design Automation | PE | 3-0-0 | 3 |
| **5.** | | CMOS Analog IC Design Lab | PC | 0-0-4 | 2 |
| **6.** | | Embedded System Design Lab | PC | 0-0-4 | 2 |
| **7.** | | Technical seminar | MC | 2-0-0 | 2 |
| **8.** | | **Audit Course – II**<br>Pedagogy Studies<br>Stress Management for Yoga Personality Development through LifeEnlightenment Skills | AC | 2-0-0 | 0 |
| **TOTAL** | | | | | **18** |

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|---|---|---|---|---|---|
| **Embedded Systems & VLSI Design (EMVL)** | | | | | |
| **Semester – III** | | | | | |
| **S.No** | **Course Code** | **Course Name** | **Category** | **L-T-P** | **Credits** |
| **1.** | | **Program Elective – V**<br>Adhoc and Wireless Sensor Networks<br>VLSI Signal Processing<br>IoT and its Applications | PE | 3-0-0 | 3 |
| **2.** | | **Open Elective**<br>Industrial Safety<br>Business Analytics<br>Waste to Energy | OE | 3-0-0 | 3 |
| **3.** | | Dissertation Phase – I | PR | 0-0-20 | 10 |
| **4.** | | Co-curricular Activities | | | 2 |
| **TOTAL** | | | | | **18** |

| Sri Krishnadevaraya University College of Engineering & Technology | | | | | |
|---|---|---|---|---|---|
| **Embedded Systems & VLSI Design (EMVL)** | | | | | |
| **Semester – IV** | | | | | |
| **S.No** | **Course Code** | **Course Name** | **Category** | **L-T-P** | **Credits** |
| **1.** | | Dissertation Phase – II | PR | 0-0-32 | 16 |
| **TOTAL** | | | | | **16** |

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| Course Code | Microcontroller Architecture and Organization | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| | Semester | I | | | |

**Course Objectives:**

- Describing the architecture of 8051 microcontroller and ARM processor
- Teaching the instruction set of 8051 and ARM microcontroller to efficient programs
- Designing system in block level using microcontroller, memory devices, buses and other peripheral devices
- Solving real life problem using microcontroller-based systems

**Course Outcomes (CO):** Student will be able to

- Describe the architectures of processors
- Develop Assembly program applying Digital logic and mathematics using 8051
- Develop Assembly Language Program ALP for ARM and ARM peripherals
- Develop ALP with minimum instructions and memory.
- Analyze and evaluate the given program in terms of code size and computational time

**UNIT - I**

**Introduction to Microcontrollers** Microprocessors Vs Microcontrollers; Classification – bits, memory architecture, ISA;
**8051 Microcontroller** Architecture – Timers, Interrupts, Register Architecture (banks), PSW register, Memory architecture; Instruction set.

**UNIT - II**

**8051 Programming and Interfaces** Programming in C & Assembly for – Interrupts, Timers and Interfaces – PORTS, LED, ADC, SENSORS, LCD, DAC, Serial Communication.

**UNIT - III**

**ARM Architecture** ARM Design Philosophy; Overview of ARM architecture; States [ARM, Thumb, Jazelle]; Registers, Modes; Conditional Execution; Pipelining; Vector Tables; Exception handling.

**UNIT - IV**

**ARM Instruction Set** ARM Instruction- data processing instructions, branch instructions, load store instructions, SWI instruction, Loading instructions, conditional Execution, Assembly Programming.

**UNIT - V**

**ARM Core based Microcontroller** Architecture of LPC214X, Memory Addressing, IO ports, Timers/counter, Watch Dog Timer, PWM, ADC/DAC, UART, Interrupts, Displays, C programming.

**Textbooks:**

1. Andrew N.Sloss, Dominic Symes, Chris Wright, ARM Developer‟s Guide, 2010, 1st Edition, Elsevier, United States
2. Kenneth Ayala, The 8051 Microcontroller & Embedded Systems Using Assembly and C, 2010, 1st edition, Cengage Learning, United States.

**Reference Books:**

1.Steve Furber ARM System on Chip Architecture, 2010, 2 nd Edition, Addison Wesley, United States
2. Technical Reference Manual CORTEX M-3, ARM, 2010, United States

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**Electronics and Communication Engineering**

| Course Code | CMOS DIGITAL IC DESIGN | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| Semester | | I | | | |

**Course Objectives:**

- To understand the fundamental properties of digital Integrated circuits using basic MOSFET equations and to develop skills for various logic circuits using CMOS related design styles.
- The course also involves analysis of performance metrics.
- To teach fundamentals of CMOS Digital integrated circuit design such as importance of Pseudo logic, Combinational MOS logic circuits and Sequential MOS logic circuits.
- To teach the fundamentals of Dynamic logic circuits and basic semiconductor memories which are the basics for the design of high performance digital integrated circuits.

**Course Outcomes (CO):** Student will be able to

- Demonstrate advanced knowledge in Static and dynamic characteristics of CMOS,
- Estimate Delay and Power of Adders circuits.
- Classify different semiconductor memories.
- Analyze, design and implement combinational and sequential MOS logic circuits.
- Analyze complex engineering problems critically in the domain of digital IC design for conducting research.
- Solve engineering problems for feasible and optimal solutions in the core area of digital ICs

**UNIT - I**

**MOS Design Pseudo NMOS Logic:** Inverter, Inverter threshold voltage, output high voltage, Output Low voltage, gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

**UNIT - II**

**Combinational MOS Logic Circuits:** MOS logic circuits with NMOS loads, Primitive CMOS logic gates–NOR & NAND gate, Complex Logic circuits design–Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

**UNIT - III**

**Sequential MOS Logic Circuits:** Behavior of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop

**UNIT - IV**

**Dynamic Logic Circuits:** Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

**UNIT - V**

**Semiconductor Memories:** Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory-NOR flash and NAND flash.

**Textbooks:**


1. Neil Weste, David Harris, "CMOS VLSI Design: A Circuits and Systems Perspective", 4th Edition, Pearson, 2010
2. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.
3. CMOS Digital Integrated Circuits Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 3rd Edition, 2011.


**Reference Books:**


1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011
2. Digital Integrated Circuits – A Design Perspective, Jan M.Rabaey, AnanthaChandrakasan, Borivoje Nikolic, 2ndEdition, PHI.

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| Course Code | COMMUNICATION BUSES AND INTERFACES<br>Program Elective – I | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| Semester | | I | | | |

**Course Objectives:**

- To understand the concepts of different types of serial buses.
- To learn about CAN, PCIe and USB architecture
- To learn about data streaming using serial communication protocols

**Course Outcomes (CO):** Student will be able to

- Understand the concepts of different types of serial buses.
- Learn about CAN, PCIe and USB architecture
- Learn about data streaming using serial communication protocols

**UNIT - I**

**Serial Busses-** Cables, Serial busses, serial versus parallel, Data and Control Signal- data frame, data rate, features, Limitations and applications of RS232, RS485, I2C , SPI

**UNIT - II**

**CAN ARCHITECTURE**- ISO 11898-2, ISO 11898-3, Data Transmission- ID allocation, Bit timing, Layers- Application layers, Object layer, Transfer layer, Physical layer, Frame formats- Dataframe, Remote frame, Error frame, Over load frame, Ack slot, Inter frame spacing, Bit spacing, Applications.

**UNIT - III**

**PCIe**
Revision, Configuration space- configuration mechanism, Standardized registers, Bus enumeration, Hardware and Software implementation, Hardware protocols, Applications.

**UNIT - IV**

**USB**
Transfer Types- Control transfers, Bulk transfer, Interrupt transfer, Isochronous transfer. Enumeration- Device detection, Default state, Addressed state, Configured state, enumeration sequencing. Descriptor types and contents- Device descriptor, configuration descriptor, Interface descriptor, Endpoint descriptor, String descriptor. Device driver.

**UNIT - V**

**Data streaming Serial Communication Protocal-** Serial Front Panel Data Port(SFPDP) configurations, Flow control, serial FPDP transmission frames, fiber frames and copper cable.

**Textbooks:**

1. A Comprehensive Guide to controller Area Network – Wilfried Voss, Copperhill Media Corporation, 2nd Ed., 2005.
2. Serial Port Complete-COM Ports, USB Virtual Com Portsand Ports for Embedded Systems- Jan Axelson, Lakeview Research, 2nd Ed.,

**Reference Books:**

1. USB Complete – Jan Axelson, Penram Publications.
2. PCI Express Technology – Mike Jackson, Ravi Budruk, Mindshare Press.

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| Course Code | DATA ACQUISITION SYSTEM DESIGN | L | T | P | C |
|---|---|---|---|---|---|
| | Program Elective – I | 3 | 0 | 0 | 3 |
| | Semester | I | | | |

**Course Objectives:**

- To understand the different types of communication interface buses.
- To familiarize different methods of ADC's and DAC's characteristics, specifications
- To studythesoftwaretoolstodevelopthecodeandimplementationfordataacquisitionsystem

**Course Outcomes (CO):** Student will be able to

Students will be able to

- Understand the different types of communication interface uses.
- Familiarize different methods of ADC's and DAC's characteristics, specifications
- Studythesoftwaretoolstodevelopthecodeandimplementationfordataacquisitionsystem

**UNIT - I**

Fundamentals of Data Acquisition Systems, Sensors and Transducers, Signal conditioning - Introduction, Types of signal conditioning, Classes of signal conditioning, DAQ Hardware, DAQ Software, Communications Cabling, Parameters of a DAQ System.

**UNIT - II**

Data acquisition system configuration, Computer plug in I/O, Distributed I/O, Stand-alone or distributed loggers/controllers- Introduction, Methods of operation, Stand-alone logger/controller hardware, firmware & software design, Communications hardware interface, Host software, Considerations, internal systems, USB overall structure, PCMCIA card

**UNIT - III**

**Data Acquisition Systems:** Hardware-Introduction, Plug-in DAQ Systems, Converters A/D, Converters D/A, Amplifier, Multiplexer/De-multiplexer, Power Management, Timing System,Filtering, Memory Board, Bus Interface.

**UNIT - IV**

Communication Bus-Bus and FireWire, Serial Communications, Wireless, Ethernet and Bluetooth, GSM for Data Acquisition System, PCI and PCI Express, Standard VME.

**UNIT - V**

**Design of Data Acquisition System:** Introduction to the Design, Functional Design of high-Speed Computers-Based DAS, Portable DAS, Design Guidelines for High-Performance Multichannel.Software for Data Acquisition Systems, Introduction to LabVIEW, Android for DAQ, Design of Firmware, Example of Implementation of a Software.

**Textbooks:**

1. Maurizio Di Paolo Emilio "Data acquisition systems-from fundamentals to applied design"springer, 2013.
2.John Park and Steve Mackay "Practical Data acquisition for instrumentation and control systems" Elsevier, 2003.

**Reference Books:**

1. Robert H King, "Introduction to Data Acquisition with LabVIEW", 2nd edition, 2012,McGraw

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**Electronics and Communication Engineering**

| Course Code | FPGA ARCHITECTURES AND APPLICATIONS | L | T | P | C |
|---|---|---|---|---|---|
| | Program Elective – I | 3 | 0 | 0 | 3 |
| | Semester | I | | | |

**Course Objectives:**

- To acquire knowledge about various architectures and device technologies of PLD's.
- To comprehend FPGA Architectures.
- To analyze System level Design and their application for Combinational and Sequential Circuits.
- To familiarize with Anti-Fuse Programmed FPGAs.
- To apply knowledge of this subject for various design applications.

**Course Outcomes (CO):** Student will be able to

- Acquire knowledge about various architectures and device technologies of PLD's.
- Comprehend FPGA Architectures.
- Analyze System level Design and their application for Combinational and SequentialCircuits.
- Familiarize with Anti-Fuse Programmed FPGAs.
- Apply knowledge of this subject for various design applications.

**UNIT - I**

**Introduction to Programmable Logic Devices:** Introduction, Simple Programmable Logic Devices – Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices–Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

**UNIT - II** **Field Programmable Gate Arrays**

**Field Programmable Gate Arrays:** Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, and Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, and Applications of FPGAs.

**UNIT - III**

**SRAM Programmable FPGAs:** Introduction, Programming Technology, Device Architecture, the Xilinx XC2000, XC3000 and XC4000 Architectures.

**UNIT - IV**

**Anti-Fuse Programmed FPGAs:** Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

**UNIT - V**

**Design Applications:** General Design Issues, Counter Examples, A Fast Video Controller, APosition Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture

**Textbooks:**


1. Field Programmable Gate Array Technology - Stephen M. Trimberger, Springer International Edition.
2. Digital Systems Design - Charles H. Roth Jr, LizyKurian John, Cengage Learning.


**Reference Books:**


1. Field Programmable Gate Arrays-John V.Oldfield, Richard C.Dorf, Wiley India.
2. Digital Design Using Field Programmable Gate Arrays - Pak K. Chan/SamihaMourad, Pearson Low Price Edition.
3. Digital Systems Design with FPGAs and CPLDs-Ian Grout, Elsevier,Newnes.
4. FPGA based System Design-Wayne Wolf, Prentice Hall Modern Semiconductor Design Series.

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**Electronics and Communication Engineering**

| Course Code | LOW POWER VLSI DESIGN | L | T | P | C |
|---|---|---|---|---|---|
| | Program Elective – II | 3 | 0 | 0 | 3 |
| | Semester | I | | | |

**Course Objectives:**

- To understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
- To implement Low power design approaches for system level and circuit level measures.
- To design low power adders, multipliers and memories for efficient design of systems.

**Course Outcomes (CO):** Student will be able to

- Understand the concepts of velocity saturation, Impact Ionization and Hot Electron Effect
- Implement Low power design approaches for system level and circuit level measures.
- Design low power adders, multipliers and memories for efficient design of systems.

**UNIT - I**

**Fundamentals:** Need for Low Power Circuit Design, Sources of Power Dissipation – Static and Dynamic Power Dissipation, Short Circuit Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

**UNIT - II**

**Low-Power Design Approaches:** Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach –Pipelining and Parallel Processing Approaches. Switched Capacitance Minimization Approaches: System Level Measures, Circuit Level Measures, Mask level Measures.

**UNIT - III**

**Low-Voltage Low-Power Adders:** Introduction, Standard Adder Cells, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low-Power Design Techniques – Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

**UNIT - IV**

**Low-Voltage Low-Power Multipliers:** Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh Wooley Multiplier, Booth Multiplier, Introductionto Wallace Tree Multiplier.

**UNIT - V**

**Low-Voltage Low-Power Memories:** Basics of ROM, Low-Power ROM Technology, Future Trendand Development of ROMs, Basics of SRAM, Memory Cell, Precharge and Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM.

**Textbooks:**

1. CMOS Digital Integrated Circuits – Analysis and Design – Sung-Mo Kang, Yusuf Leblebici, TMH, 2011.
2. Low-Voltage, Low-Power VLSI Subsystems – Kiat-Seng Yeo, Kaushik Roy, TMH Professional Engineering.

**Reference Books:**

1. Introduction to VLSI Systems: A Logic, Circuit and System Perspective – Ming-BO Lin, CRC Press, 2011.
2.Low Power CMOS Design – AnanthaChandrakasan, IEEE Press/Wiley International, 1998.
3. Low Power CMOS VLSI Circuit Design – Kaushik Roy, Sharat C. Prasad, John Wiley & Sons, 2000.

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| Course Code | NANOMATERIALS AND NANOTECHNOLOGY | L | T | P | C |
|---|---|---|---|---|---|
| | Program Elective – II | 3 | 0 | 0 | 3 |
| Semester | | I | | | |

**Course Objectives:**

- To understand the basic idea behind the design and fabrication of nano scale systems.
- To understand and formulate new engineering solutions for current problems and technologies for future applications.
- To acquire knowledge on the operation of fabrication and characterization devices to achieve precisely designed systems.

**Course Outcomes (CO):** Student will be able to

- Understand the basic science behind the design and fabrication of nano scale systems.
- Understand and formulate new engineering solutions for current problems and competing technologies for future applications.
- Make inter disciplinary projects applicable to wide areas by clearing and fixing the boundaries in system development.
- Gather detailed knowledge of the operation of fabrication and characterization devices to achieve precisely designed systems.

**UNIT - I**

Introduction of nano materials and nanotechnologies, Features of nanostructures, Applications of nano materials and technologies. Nano dimensional Materials 0D, 1D, 2D structures – Size Effects – Fraction of Surface Atoms –Specific Surface Energy and Surface Stress – Effect on the Lattice Parameter – Phonon Density of States – the General Methods available for the Synthesis of Nanostructures – precipitate – reactive– hydrothermal/solvo thermal methods – suitability of such methods for scaling – potential Uses.

**UNIT - II**

Fundamentals of nanomaterials, Classification, Zero-dimensional nanomaterials, One-dimensional nanomaterials, Two-dimensional nano materials, three dimensional nanomaterials. Low Dimensional Nanomaterials and its Applications, Synthesis, Properties and applications of Low Dimensional Carbon-Related Nanomaterials.

**UNIT - III**

Micro- and Nanolithography Techniques, Emerging Applications, Introduction to Micro electro mechanical Systems (MEMS), Advantages and Challenges of MEMS, Fabrication Technologies, Surface Micromachining, Bulk Micromachining, Molding. Introduction to Nano Phonics.

**UNIT - IV**

Introduction, Synthesis of CNTs - Arc-discharge, Laser-ablation, Catalytic growth, Growth mechanisms of CNT‟s - multi-walled nanotubes, Single-walled nano tubes Optical properties of CNT‟s, Electrical transport in perfect nanotubes, Applications as case studies. Synthesis and Applications of CNTs.

**UNIT - V**

Ferroelectric materials, coating, molecular electronics and Nano electronics, biological and environmental, membrane-based application, polymer-based application.

**Textbooks:**


1. Kenneth J.Klabunde and Ryan M.Richards, “Nanoscale Materials in Chemistry”, 2ndedition,John Wiley and Sons, 2009.
2. I Gusev and A Rempel, “Nanocrystalline Materials”, Cambridge International Science Publishing, 1stIndian edition by Viva Books Pvt. Ltd. 2008.
3. B.S.Murty,P.Shankar,Baldev Raj, B.B.Rath, James Murday, “Nanoscience and Nanotechnology”, Tata McGrawHill Education 2012.



| **Reference Books:** |
|---|
| 1. Digital Integrated Circuit Design – Ken Martin, Oxford University Press, 2011.<br>2. Digital Integrated Circuits - A Design Perspective, Jan M.Rabaey, AnantChandrakasan, Borvivoje Nikolic, 2nd Edition, PHI. |

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**Electronics and Communication Engineering**

| Course Code | NETWORK SECURITY AND CRYPTOGRAPHY | L | T | P | C |
|---|---|---|---|---|---|
| | Program Elective – II | 3 | 0 | 0 | 3 |
| | Semester | I | | | |

**Course Objectives:**

- To identify and utilize different forms of cryptography techniques.
- To incorporate authentication and security in the network applications.
- To distinguish among different types of threats to the system and handle the same.

**Course Outcomes (CO):**

- Identify and utilize different forms of cryptography techniques.
- Incorporate authentication and security in the network applications.
- Distinguish among different types of threats to the system and handle the same.

**UNIT - I**

**Security:** Need, security services, Attacks, OSI Security Architecture, one-time passwords, Model for Network security, Classical Encryption Techniques like substitution ciphers, Transposition ciphers, Cryptanalysis of Classical Encryption Techniques.

**UNIT - II**

**Number Theory**: Introduction, Fermat's and Euler's Theorem, The Chinese Remainder Theorem, Euclidean Algorithm, Extended Euclidean Algorithm, and Modular Arithmetic.

**UNIT - III**

**Private-Key (Symmetric) Cryptography**: Block Ciphers, Stream Ciphers, RC4 Stream cipher, Data Encryption Standard (DES), Advanced Encryption Standard (AES), Triple DES, RC5, IDEA, Linear and Differential Cryptanalysis.

**UNIT - IV**

**Public-Key (Asymmetric) Cryptography**: RSA, Key Distribution and Management, Diffie-Hellman Key Exchange, Elliptic Curve Cryptography, Message Authentication Code, hash functions, message digest algorithms: MD4 MD5, Secure Hash algorithm, RIPEMD-160, HMAC.

**UNIT - V**

**Authentication and System Security**: IP and Web Security Digital Signatures, Digital Signature Standards, Authentication Protocols, Kerberos, IP security Architecture, Encapsulating Security Payload, Key Management, Web Security Considerations, Secure Socket Layer, Secure Electronic Transaction Intruders, Intrusion Detection, Password Management, Worms, viruses, Trojans, Virus Countermeasures, Firewalls, Trusted Systems.

**Textbooks:**

1. William Stallings, "Cryptography and Network Security, Principles and Practices", Pearson Education, 3rd Edition.
2. Charlie Kaufman, Radia Perlman and Mike Speciner, "Network Security, Private Communication in a Public World", Prentice Hall, 2ND Edition.

**Reference Books:**

1. Christopher M. King, ErtemOsmanoglu, Curtis Dalton, "Security Architecture, Design Deployment and Operations", RSA Pres,
2. Stephen Northcutt, LenyZeltser, Scott Winters, Karen Kent, and Ronald W. Ritchey, "Inside Network Perimeter Security", Pearson Education, 2 ndEdition
3. Richard Bejtlich, "The Practice of Network Security Monitoring: Understanding Incident Detection and Response", William Pollock Publisher, 2013.

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| Course Code | CMOS DIGITAL IC DESIGN LAB | L | T | P | C |
|---|---|---|---|---|---|
| | | 0 | 0 | 4 | 2 |
| Semester | | I | | | |

**Course Objectives:**

- To explain the VLSI Design Methodologies using any VLSI design tool.
- To grasp the significance of various design logic Circuits in full-custom IC Design.
- To explain the Physical Verification in Layout Extraction.
- To fully appreciate the design and analyze of CMOS Digital Circuits.
- To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

**Course Outcomes (CO):**

- Explain the VLSI Design Methodologies using any VLSI design tool.
- Grasp the significance of various design logic Circuits in full-custom IC Design.
- Explain the Physical Verification in Layout Extraction.
- Fully appreciate the design and analyze of CMOS Digital Circuits. Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation.

**List of Experiments**:

The students are required to design and implement the Circuit and Layout of any **TEN** Experiments using CMOS 130nm Technology.

1. Inverter Characteristics.
2. NAND and NOR Gate
3. XOR and XNOR Gate
4. 2:1 Multiplexer
5. Full Adder
6. RS-Latch
7. Clock Divider
8. JK-Flip Flop
9. Synchronous Counter
10. Asynchronous Counter11.Static RAM Cell
12. Dynamic Logic Circuits
13. Linear Feedback Shift Register

**Lab Requirements:**

**Software:**

Mentor Graphics Tool/ Cadence/ Synopsys/Industry Equivalent Standard Software

**Hardware:**

Personal Computer with necessary peripherals, configuration and operating System.

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| Course Code | MICROCONTROLLERS LAB | L | T | P | C |
|---|---|---|---|---|---|
| | | 0 | 0 | 4 | 2 |
| Semester | | I | | | |

**Course Objectives:**

- To write the ARM 'C' programming for applications
- To understand the interfacing of various modules with ARM 7/ ARM Cortex-M3
- To develop assembly and C Programming for DSP processors

**Course Outcomes (CO):**

- Install, configure and utilize tool sets for developing applications based on ARM processor core.
- Design and developtheARM7 based embedded systems for various applications.
- Develop application programs on ARM and DSP development boards both in assembly andC.
- Design and Implement the digital filters on DSP6713 processor.
- Analyze the hardware and software interaction and integration.

**List of Experiments**:

**Part** Experiments to be carried out on Cortex-Mx development boards and using GNU tool-chain

1. Blink an LED with software delay, delay generated using the SysTick timer.
2. System clock real time alteration using the PLL modules.
3. Control intensity of an LED using PWM implemented in software and hardware.
4. Control an LED using switch by polling method, by interrupt method and flash the LED onceevery five switch presses.
5. UART Echo Test.
6. Take analog readings on rotation of rotary potentiometer connected to an ADC channel.
7. Temperature indication on an RGB LED.
8. Mimic light intensity sensed by the light sensor by varying the blinking rate of an LED.
9. Evaluate the various sleep modes by putting core in sleep and deep sleep modes.
10. System reset using watchdog timer in case something goes wrong.
11. Sample sound using a microphone and display sound levels on LEDs.

**Software Requirements:**
Keil for ARM, Code Composer Studio
**Hardware Requirements:**
ARM Cortex Mx Development Boards,

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**Electronics and Communication Engineering**

| Course Code | RESEARCH METHODOLOGY AND IPR | L | T | P | C |
|---|---|---|---|---|---|
| | | 2 | 0 | 0 | 2 |
| Semester | | I | | | |

**Course Objectives:**

- Identify an appropriate research problem in their interesting domain.
- Understand ethical issues understand the Preparation of a research project thesis report.
- Understand the Preparation of a research project thesis report
- Understand the law of patent and copyrights.
- Understand the Adequate knowledge on IPR

**Course Outcomes (CO):** Student will be able to

- Analyze research related information
- Follow research ethics
- Understand that today's world is controlled by Computer, Information Technology, but tomorrow world will be ruled by ideas, concept, and creativity.
- Understanding that when IPR would take such important place in growth of individuals & nation, it is needless to emphasis the need of information about Intellectual Property Right to be promoted among students in general & engineering in particular.
- Understand that IPR protection provides an incentive to inventors for further research work and investment in R & D, which leads to creation of new and better products, and in turn brings about, economic growth and social benefits.

**UNIT - I**

Meaning of research problem, Sources of research problem, Criteria Characteristics of a good research problem, Errors in selecting a research problem, scope, and objectives of research problem. Approaches of investigation of solutions for research problem, data collection, analysis, interpretation, Necessary instrumentations

**UNIT - II**

Effective literature studies approaches, analysis Plagiarism, Research ethics, Effective technical writing, howto write report, Paper Developing a Research Proposal, Format of research proposal, a presentation and assessment by a review committee.

**UNIT - III**

Nature of Intellectual Property: Patents, Designs, Trade and Copyright. Process of Patenting and Development: technological research, innovation, patenting, development. International Scenario: International cooperation on Intellectual Property. Procedure for grants of patents, Patenting under PCT.

**UNIT - IV**

Patent Rights: Scope of Patent Rights. Licensing and transfer of technology. Patent information and databases. Geographical Indications.

**UNIT - V**

New Developments in IPR: Administration of Patent System. New developments in IPR; IPR of Biological Systems, Computer Software etc. Traditional knowledge Case Studies, IPR and IITs.

**Textbooks:**

1. Stuart Melville and Wayne Goddard, "Research methodology: an introduction for science & engineering students'"
2. Wayne Goddard and Stuart Melville, "Research Methodology: An Introduction"

**Reference Books:**

1. Ranjit Kumar, 2nd Edition, "Research Methodology: A Step-by-Step Guide for beginners"
2. Halbert, "Resisting Intellectual Property", Taylor & Francis Ltd ,2007.
3. Mayall, "Industrial Design", McGraw Hill, 1992.
4. Niebel, "Product Design", McGraw Hill, 1974.
5. Asimov, "Introduction to Design", Prentice Hall, 1962.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, "Intellectual Property in NewTechnological Age", 2016.

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**Electronics and Communication Engineering**

| Course Code | CMOS ANALOG IC DESIGN | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| Semester | | II | | | |

**Course Objectives:**

- This course focuses on theory, analysis and design of analog integrated circuits in both Bipolar and Metal-Oxide-Silicon (MOS) technologies.
- Basic design concepts, issues and tradeoffs involved in analog IC design are explored.
- Intuitive understanding and real-life applications are emphasized throughout the course.
- To learn about Design of CMOS Op Amps, Compensation of Op Amps, Design of Two- Stage Op Amps, Power Supply Rejection Ratio of Two-Stage Op Amps, Cascade Op Amps, Measurement Techniques of OP Amp.

**Course Outcomes (CO):** Student will be able to

- Design MOSFET based analog integrated circuits.
- Analyze analog circuits at least to the first order.
- Appreciate the trade-offs involved in analog integrated circuit design.
- Understand and appreciate the importance of noise and distortion in analog circuits.
- Analyze complex engineering problems critically in the domain of analog IC design for conducting research.

**UNIT - I**

**Basic MOS Device Physics:** General Considerations, MOS I/V Characteristics, Second Order effects, MOS Device models and MOS Capacitor. Short Channel Effects and Device Models. Single Stage Amplifiers – Basic Concepts, Common Source Stage, Source Follower, Common Gate Stage, Cascode Stage.

**UNIT - II**

**Differential Amplifiers:** Single Ended and Differential Operation, Basic Differential Pair, Common Mode Response, Differential Pair with MOS loads, Gilbert Cell. Passive and Active Current Mirrors – Basic Current Mirrors, Cascode Current Mirrors, Active Current Mirrors. Current Steering Circuit

**UNIT - III**

**Frequency Response of Amplifiers:** General Considerations, Common Source Stage, SourceFollowers, Common Gate Stage, Cascode Stage, Differential Pair. Noise – Types of Noise, Representation of Noise in circuits, Noise in single stage amplifiers, Noise in Differential Pairs.

**UNIT - IV**

**Feedback Amplifiers:** General Considerations, Feedback Topologies, Effect of Loading. Operational Amplifiers – General Considerations, One Stage Op Amps, Two Stage Op Amps, Gain Boosting, Common – Mode Feedback, Input Range limitations, Slew Rate, Power Supply Rejection, Noise in Op Amps, Stability and Frequency Compensation.

**UNIT - V**

**Comparators:** Characterization of comparator, Two-Stage, Open-Loop comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.

**Textbooks:**

1. B.Razavi, "Design of Analog CMOS Integrated Circuits", 2nd Edition, McGraw Hill Edition2016.
Paul.R.Gray& Robert G. Meyer, "Analysis and Design of Analog Integrated Circuits", Wiley, 5th Edition, 2009.

**Reference Books:**

1.T.C. Carusone, D.A.Johns &K.Martin, "Analog Integrated Circuit Design", 2nd Edition, Wiley, 2012.
2. P.E.Allen&D.R.Holberg, "CMOS Analog Circuit Design", 3rd Edition, Oxford University Press, 2011.
3. R.Jacob Baker, "CMOS Circuit Design, Layout, and Simulation", 3rd Edition, Wiley, 2010.
4. Adel S. Sedra, Kenneth C. Smith, Arun, "Microelectronic Circuits", 6th Edition, Oxford University Press

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**Electronics and Communication Engineering**

| Course Code | EMBEDDED SYSTEMS DESIGN | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| Semester | | II | | | |

**Course Objectives:**

- To differentiate between a General purpose and an Embedded System.
- To provide knowledge on the building blocks of Embedded System.
- To understand the requirement of Embedded firmware and its role in API.

**Course Outcomes (CO):** Student will be able to

- Expected to differentiate the design requirements between General Purpose and Embedded Systems.
- Expected to acquire the knowledge of firmware design principles.
- Expected to understand the role of Real Time Operating System in Embedded Design.
- To acquire the knowledge and experience of task level Communication in any Embedded System.

**UNIT - I**

Introduction to Embedded Systems: Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems,
Characteristics and Quality Attributes of Embedded Systems.

**UNIT - II**

Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS), Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces. DDR , Flash, NVRAM

**UNIT - III**

Embedded Firmware: Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer, Embedded Firmware Design Approaches and Development Languages.

**UNIT - IV**

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems,Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

**UNIT - V**

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

**Textbooks:**

1. Introduction to Embedded Systems - Shibu K.V, Mc Graw Hill.

**Reference Books:**

1. Embedded Systems - Raj Kamal, TMH.
2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.
3. Embedded Systems – Lyla, Pearson, 2013
4. An Embedded Software Primer - David E. Simon, Pearson Education.

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**Electronics and Communication Engineering**

| Course Code | PATTERN RECOGNITION AND MACHINE LEARNING | L | T | P | C |
|---|---|---|---|---|---|
| | Program Elective – III | 3 | 0 | 0 | 3 |
| Semester | | II | | | |

**Course Objectives:**

- To understand the mathematical formulation of patterns.
- To study the various linear models.
- To understand the basic classifiers.
- To distinguish different models.

**Course Outcomes (CO):**

Student will be able to

- Learn the basics of pattern classes and functionality.
- Construct the various linear models.
- Understand the importance kernel methods.
- Learn the Markov and Mixed models.

**UNIT - I**

**Introduction to Pattern recognition:** Mathematical Formulation and Basic Functional Equation, Reduction of Dimensionality, Experiments in Pattern Classification, Backward Procedure for Both Feature Ordering- and Pattern Classification, Suboptimal Sequential Pattern Recognition, Nonparametric Design of Sequential Pattern Classifiers, Analysis of Optimal Performance and a Multiclass Generalization

**UNIT - II**

**Linear Models:** Linear Basis Function Models -Maximum likelihood and least squares, Geometry of least squares , Sequential learning, Regularized least squares, Multiple outputs , The Bias-Variance Decomposition, Bayesian Linear Regression -Parameter distribution, Predictive, Equivalent, Bayesian Model Comparison, Probabilistic Generative Models-Continuous inputs , Maximum likelihood solution, Discrete features, Exponential family, Probabilistic Discriminative Models - Fixed basis functions, Logistic regression, Iterative reweighted least squares, Multiclass logistic regression, Probit regression, Canonical link functions

**UNIT - III**

**Kernel Methods**: Constructing Kernels, Radial Basis Function Networks - Nadaraya-Watson model, Gaussian Processes -Linear regression revisited, Gaussian processes for regression, Learning the hyper parameters, Automatic relevance determination, Gaussian processes for classification, Laplace approximation, Connection to neural networks, Sparse Kernel Machines- Maximum Margin Classifiers, Overlapping class distributions, Relation to logistic regression, Multiclass SVMs, SVMs for regression, Computational learning theory, Relevance Vector Machines- RVM for regression, Analysis of sparsity, RVM for classification

**UNIT - IV**

**Graphical Models**: Bayesian Networks, Example: Polynomial regression, Generative models, Discrete variables, Linear-Gaussian models, Conditional Independence- Three example graphs, Dseparation, Markov Random Fields -Conditional independence properties, Factorization properties, Illustration: Image de-noising, Relation to directed graphs, Inference in Graphical Models- Inference on a chain, Trees, Factor graphs, The sum-product algorithm, The max-sum algorithm, Exact inference in general graphs, Loopy belief propagation, Learning the graph structure.

**UNIT - V**

**Mixture Models and EM algorithm:** K-means Clustering-Image segmentation and compression, Mixtures of Gaussians-Maximum likelihood, EM for Gaussian mixtures, An Alternative View of EM Gaussian mixtures revisited, Relation to K-means, Mixtures of Bernoulli distributions, EM for Bayesian linear regression, The EM Algorithm in General, Combining Models- Tree-based Models, Conditional Mixture Models- Mixtures of linear regression models, Mixtures of logistic models, Mixtures of experts.



| **Textbooks:** |
|---|
| 1. Sequential methods in Pattern Recognition and Machine Learning-K.S.Fu, Academic Press,volume no.52.<br>2. Pattern Recognition and Machine Learning- C. Bishop-Springer,2006. |
| **Reference Books:** |
| 1. Pattern Classification- Richard o. Duda, Peter E. hart, David G. Stork, John Wiley& Sons, 2nd Ed., 2001.<br>2. The elements of Statistical Learning- Trevor Hastie, Robert Tibshirani, Jerome H. Friedman, Springer, 2nd Ed., 2009 |

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**Electronics and Communication Engineering**

| Course Code | PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE<br>Program Elective – III | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| Semester | | II | | | |

**Course Objectives:**

- To introduce students to various programming languages like C, C++,Java script, PERL, etc.
- To distinguish between Procedural and OOP language, Introduce features of OOPs etc.
- To demonstrate the development of some typical applications using different Programming languages.

**Course Outcomes (CO):**

Students will be able to:

- Introduce students to various programming languages like C, C++,Java script, PERL, etc.
- Distinguish between Procedural and OOP language, Introduce features of OOPs etc.
- Demonstrate the development of some typical applications using different Programming languages.

**UNIT - I**

**Embedded 'C' Programming:** Bitwise operations, Dynamic memory allocation, OS services, linked stack and queue, Sparse matrices, Binary tree, Interrupt handling in C, Code optimizationissues, Writing LCD drives, LED drivers, Drivers for serial port communication, Embedded
Software Development Cycle and Methods (Waterfall, Agile).

**UNIT - II**

**Object Oriented Programming:** Introduction to procedural, modular, object oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data
Abstraction and information hiding, inheritance, polymorphism.

**UNIT - III**

**CPP Programming:** 'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function,
dynamic memory allocation.

**UNIT - IV**

**Overloading and Inheritance:** Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friendclasses, types of inheritance, hybrid inheritance,
multiple inheritance.
Templates: Function template and class template, member function templates and template arguments

**UNIT - V**

**Exception Handling**: Syntax for exception handling code: try-catch-throw, Multiple Exceptions.
**Scripting Languages**: Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL: Operators, Statements Pattern Matching etc. Data Structures, Modules, Objects, Tied
Variables, Inter process Communication Threads, Compilation & Line Interfacing.

**Textbooks:**

1. Michael J. Pont , "Embedded C", Pearson Education, 2ndEdition,2008
2.Robert Sedgewick, "Algorithms in C++", Addison Wesley PublishingCompany, 1999.

**Reference Books:**

1. Randal L. Schwartz, "Learning Perl", O'Reilly Publications, 6th Edition20112.Michael Berman, "Data structures via C++", Oxford UniversityPress, 2002

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**Electronics and Communication Engineering**

| Course Code | RF IC DESIGN | L | T | P | C |
|---|---|---|---|---|---|
| | Program Elective – III | 3 | 0 | 0 | 3 |
| Semester | | II | | | |

**Course Objectives:**

- To introduce students the concept of tuned circuit, matching network, reflection coefficients, transmission lines and MOS high frequency behavior etc.
- To demonstrate design of High Frequency Amplifiers.
- To introduce various types of Power Amplifiers and PLLs

**Course Outcomes (CO):**

Students will be able to

- Introduce students the concept of tuned circuit, matching network, reflection coefficients, transmission lines and MOS high frequency behavior etc.
- Demonstrate design of High Frequency Amplifiers.
- Introduce various types of Power Amplifiers and PLLs

**UNIT - I**

**RF Tuned Circuits:** RF systems – Basic architectures, Maximum Power Transfer, Passive RLC Networks, Parallel RLC tank, Q, Series RLC networks, matching, Pi match, T match, Passive components in IC: Resistors, capacitors, Inductors, Transceiver Architectures.

**UNIT - II**

**Nonlinearity and Reflection Coefficient:** Nonlinearity and Time Variance of system, sensitivity and dynamic range, Review of MOS Device Physics, MOS device review, Distributed Systems, Transmission lines, reflection coefficient, the wave equation Lossy transmission lines Smith charts – plotting gamma, Noise in FET: Thermal noise, flicker noise review

**UNIT - III**

**High Frequency Amplifier Design:** Bandwidth estimation using open-circuit time constants, Bandwidth estimation using short-circuit time constants, Rise-time, delay and bandwidth, Zeros to enhance bandwidth, Shunt- series amplifiers, tuned amplifiers Cascaded amplifiers, Noise figure, Intrinsic MOS noise parameters, LNA Design, Power match versus noise match.

**UNIT - IV**

**RF Power Amplifiers:** Multiplier based mixers, Subsampling mixers & Mixer Design, RF PowerLarge signal performance Amplifiers, Class A, AB, B, C amplifiers, Class D, E, F amplifiers, RF Power amplifier design issues.

**UNIT - V**

**PLL:** Voltage controlled oscillators, Resonators, Negative resistance oscillators, Phase locked loops, Linearized PLL models, Phase detectors, charge pumps, Loop filters, PLL design examples, Frequency synthesis and oscillator Frequency division, integer-N synthesis, Fractional frequency synthesis, Phase noise.

**Textbooks:**

1. Thomas H. Lee, “The Design of CMOS Radio-Frequency Integrated Circuits”, Cambridge University Press, 2004.

| |
|---|
| 2.BehzadRazavi, "RF Microelectronics", Prentice Hall, 1997. |
| **Reference Books:** |
| 1. Abidi, P.R. Gray, and R.G. Meyer, eds., "Integrated Circuits for Wireless Communications", New York: IEEE Press, 1999.<br>2.R. Ludwig and P. Bretchko, "RF Circuit Design, Theory andApplications", Pearson, 2000 |

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**Electronics and Communication Engineering**

| Course Code | SoC ARCHITECTURE | L | T | P | C |
|---|---|---|---|---|---|
| | Program Elective – IV | 3 | 0 | 0 | 3 |
| Semester | | II | | | |

**Course Objectives:**

- To understand the basics related to SoC architecture and different approaches related to SoC Design.
- To select an appropriate robust processor for SoC Design
- To select an appropriate memory for SoC Design.
- To realize real time case studies

**Course Outcomes (CO):** Student will be able to

- Understand the basics related to SoC architecture and different approaches related to SoC Design.
- Select an appropriated robust processor for SoC Design
- Select an appropriate memory for SoC Design.
- Realize real time case studies

**UNIT - I**

**Introduction to the System Approach:** System Architecture, Components of the system, Hardware& Software, Processor Architectures, Memory &Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity.

**UNIT - II**

**Processors:** Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Microarchitecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors andVector Instruction extensions, VLIW Processors, Superscalar Processors

**UNIT - III**

**Memory Design for SOC:** Overview: SOC external memory, SOC Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Other Types of Cache, Split – I, and D – Caches, MultilevelCaches, SOC Memory System, Models of Simple Processor – memory interaction.

**UNIT - IV**

**Interconnect, Customization and Configurability:** Interconnect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bustransactions and contention time.

**SOC Customization:** An overview, Customizing Instruction Processor, Reconfigurable Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

**UNIT - V**

**Application Studies / Case Studies:** SOC Design approach; AES-algorithms, Design and evaluation; Image compression–JPEG compression.

**Textbooks:**

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber, 2ndEdition, 2000, Addison Wesley Professional.

**Reference Books:**



1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer 2.Co-Verification of Hardware and Software for ARM System on Chip Design (EmbeddedTechnology) – Jason Andrews – Newnes, BK and CDROM.
3.System on Chip Verification – Methodologies and Techniques –PrakashRashinkar, PeterPaterson and Leena Singh L, 2001, Kluwer Academic Publishers

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**Electronics and Communication Engineering**

| Course Code | SYSTEM DESIGN WITH EMBEDDED LINUX | L | T | P | C |
|---|---|---|---|---|---|
| | Program Elective – IV | 3 | 0 | 0 | 3 |
| Semester | | II | | | |

**Course Objectives:**

- To understand the importance of Embedded Linux in system design
- To analyze the architecture of embedded Linux in detail
- To explain the Linux BSP for a hardware platform
- To develop and Debug the drivers in Embedded Linux

**Course Outcomes (CO):**

Students will be able to

- Understand the importance of Embedded Linux in system design
- Analyze the architecture of embedded Linux in detail
- Explain the Linux BSP for a hardware platform
- Develop and Debug the drivers in Embedded Linux

**UNIT - I**

**Introduction:** Need of Embedded Linux, Embedded Linux versus Desktop Linux, Embedded Linux Distributions Embedded Linux Architecture, Kernel Architecture: Hardware Abstraction Layer (HAL), Memory Manager, Scheduler, File System, IO Subsystem, Networking Subsystems, IPC;
User Space, Linux Start-Up Sequence.

**UNIT - II**

**Board Support Package:** Inserting BSP in Kernel Build Procedure, the Boot Loader Interface, Memory Map, Interrupt Management, the PCI Subsystem, Timers, UART, and Power Management. Embedded Storage: Flash Map, Memory Technology Device, MTD Architecture, Embedded File Systems.

**UNIT - III**

**Embedded Drivers:** Linux Serial Driver, Ethernet Driver, and I2C Subsystem on Linux, USB Gadgets, Watchdog Timer, and Kernel Modules. Porting Applications: Architectural Comparison, Application Porting Roadmap.

**UNIT - IV**

**Real-Time Linux:** Linux and Real-Time: Building and Debugging: Building the Kernel, Buildingthe Root File System, Integrated Development Environment, Elementary Concepts of Debugging. Embedded Graphics: Graphics System, Introduction to Display Hardware.

**UNIT - V**

**uClinux:** Linux on MMU - Less Systems, Program Load and Execution, Memory Management, File / Memory Mapping.

**Textbooks:**

1. Derek Molloy, “Exploring Beagle Bone: Tools and Techniques for Building with EmbeddedLinux”, Wiley, 1st Edition, 2014.
2.Christopher Hallinan, “Embedded Linux Primer: A Practical Real-World Approach”, Prentice Hall, 2nd Edition, 2010.

**Reference Books:**

1. P Raghvan, Amol Lad, SriramNeelakandan, “EmbeddedLinux System Design and Development”, Auerbach Publications, 2005.
2.KarimYaghmour, “Building Linux Systems”, O’Reilly & Associates,2008.

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**Electronics and Communication Engineering**

| Course Code | PHYSICAL DESIGN AUTOMATION | L | T | P | C |
|---|---|---|---|---|---|
| | Program Elective – IV | 3 | 0 | 0 | 3 |
| | Semester | II | | | |

**Course Objectives:**

- To understand relation between automation algorithms and constraints posed by VLSI technology.
- To adopt algorithms to meet critical design parameters.
- To design area efficient logics by employing different routing algorithms and shape functions.
- To simulate and synthesis different combinational and sequential logics.

**Course Outcomes (CO):** Student will be able to

- Understand relation between automation algorithms and constraints posed by VLSI technology.
- Adopt algorithms to meet critical design parameters.
- Design area efficient logics by employing different routing algorithms and shape functions.
- Simulate and synthesis different combinational and sequential logics.

**UNIT - I**

**VLSI Design Automation Tools:** Algorithms and system design, Structural and logic design, Transistor level design, Layout design, Verification methods, Design management tools.

**UNIT - II**

**Layout:** Compaction, placement and routing, Design rules, symbolic layout, Applications of compaction. Formulation methods, Algorithms for constrained graph compaction, Circuit representation, Wire length estimation, Placement algorithms, Partitioning algorithms.

**UNIT - III**

**Floor planning and routing:** Floor planning concepts, Shape functions and floor planning sizing, Local routing, Area routing, Channel routing, global routing and its algorithms.

**UNIT - IV**

**Simulation and Logic Synthesis:** Gate level and switch level modeling and simulation, Introduction to combinational logic synthesis, ROBDD principles, implementation, construction and manipulation, Two level logic synthesis.

**UNIT - V**

**High-Level Synthesis:** Hardware model for high level synthesis, internal representation of input algorithms, Allocation, assignment and scheduling, scheduling algorithms, Aspects of assignment, High level transformations.

**Textbooks:**

1. S.H. Gerez, Algorithms for VLSI Design Automation, John Wiley, 1998.
2. N.A. Sherwani, Algorithms for VLSI Physical Design Automation, (3/e), Kluwer, 1999.

**Reference Books:**

1. S.M. Sait,H.Youssef, VLSI Physical Design Automation, World scientific, 1999.
2. M.Sarrafzadeh, Introduction to VLSI Physical Design, McGraw Hill (IE), 1996

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| Course Code | CMOS ANALOG IC DESIGN LAB | L | T | P | C |
|---|---|---|---|---|---|
| | | 0 | 0 | 4 | 2 |
| Semester | | II | | | |

**Course Objectives:**

- To explain the VLSI Design Methodologies using VLSI design tool.
- To grasp the significance of various CMOS analog circuits in full-custom IC Design flow
- To explain the Physical Verification in Layout Design
- To fully appreciate the design and analyze of analog and mixed signal simulation
- To grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

**Course Outcomes (CO):**

- Explain the VLSI Design Methodologies using VLSI design tool.
- Grasp the significance of various CMOS analog circuits in full-custom IC Design flow
- Explain the Physical Verification in Layout Design
- Fully appreciate the design and analyze of analog and mixed signal simulation
- Grasp the Significance of Pre-Layout Simulation and Post-Layout Simulation

**List of Experiments**:

- The students are required to design and implement any **TEN** Experiments using CMOS 130nm Technology.
- The students are required to implement LAYOUTS of any **SIX** Experiments using CMOS 130nm Technology and Compare the results with Pre-Layout Simulation.

1. MOS Device Characterization and parametric analysis
2. Common Source Amplifier
3. Common Source Amplifier with source degeneration
4. Cascode amplifier
5. Simple current mirror
6. Cascode current mirror.
7. Wilson current mirror.
8. Differential Amplifier
9. Operational Amplifier
10. Sample and Hold Circuit
11. Direct-conversion ADC
12. R-2R Ladder Type DAC

**Lab Requirements:**
**Software:**
Mentor Graphics – Pyxis Schematic, IC Station, Calibre, ELDO Simulator
**Hardware:**
Personal Computer with necessary peripherals, configuration and operating System.

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**Electronics and Communication Engineering**

| Course Code | EMBEDDED SYSTEM DESIGN LAB | L | T | P | C |
|---|---|---|---|---|---|
| | | 0 | 0 | 4 | 2 |
| Semester | | II | | | |

**Course Objectives:**

- To familiarize with embedded systems programming concepts
- To implement different embedded communication and interfacing protocols

**Course Outcomes (CO):**

- Familiarize with embedded systems programming concepts
- Implement different embedded communication and interfacing protocols

**List of Experiments**:

1. Functional Testing of Devices
Flashing the OS on to the device into a stable functional state by porting desktop environment with necessary packages.
2. Exporting Display on to other Systems
Making use of available laptop/desktop displays as a display for the device using SSH client & X11 display server.
3. GPIO Programming
Programming of available GPIO pins of the corresponding device using native programming language. Interfacing of I/O devices like LED/Switch etc., and testing the functionality.
4. Interfacing Chronos eZ430
Chronos device is a programmable Texas Instruments watch which can be used for multiple purposes like PPT control, Mouse operations etc., Exploit the features of the device by interfacingwith devices.
5. ON/OFF Control Based On Light Intensity
Using the light sensors, monitor the surrounding light intensity & automatically turn ON/OFF thehigh intensity LED's by taking some pre-defined threshold light intensity value.
6. Battery Voltage Range Indicator
Monitor the voltage level of the battery and indicating the same using multiple LED's (for ex: for 3V battery and 3 LEDs, turn on 3 LED s for 2-3V, 2 LEDs for 1-2V, 1 LED for 0.1-1V & turn offall for 0V)
7. Dice Game Simulation
Instead of using the conventional dice, generate a random value similar to dice value and display the same using a 16X2 LCD. A possible extension could be to provide the user with option of selecting single or double dice game.
8. Displaying RSS News Feed On Display Interface
Displaying the RSS news feed headlines on a LCD display connected to device. This can be adaptedto other websites like twitter or other information websites. Python can be used to acquire data fromthe internet.
9. Porting Open w.r.t the Device
Attempt to use the device while connecting to a WiFi network using a USB dongle and at the same time providing a wireless access point to the dongle.
10. Hosting a website on Board
Building and hosting a simple website(static/dynamic) on the device and make it accessible online. There is a need to install server (eg: Apache) and thereby host the website.
11. Webcam Server

Interfacing the regular USB webcam with the device and turn it into fully functional IP webcam & test the functionality.

12. FM Transmission

Transforming the device into a regular FM transmitter capable of transmitting audio at desired frequency (generally 88-108 Mhz)

**Software Requirements:**

Keil / Python

**Hardware Requirements:**

Arduino/Raspbery Pi/Beaglebone

**Sri Krishnadevaraya University College of Engineering & Technology**
**Ananthapuramu-515003(A.P) India**
**Electronics and Communication Engineering**

| Course Code | ADHOC AND WIRELESS SENSOR NETWORKS | L | T | P | C |
|---|---|---|---|---|---|
| | Program Elective – V | 3 | 0 | 0 | 3 |
| Semester | | III | | | |

**Course Objectives:**

- To understand the various wireless networks
- To analyze MAC, routing and transport layer protocols
- To learn about the concepts of wireless sensor networks

**Course Outcomes (CO):**

Students will be able to

- Understand the various wireless networks
- Analyze MAC, routing and transport layer protocols
- Learn about the concepts of wireless sensor networks

**UNIT - I**

**Wireless LANs and PANs**: Introduction, Fundamentals of WLANS, IEEE 802.11 Standards, HIPERLAN Standard, Bluetooth, Home RF.
**AD HOC WIRELESS NETWORKS**: Introduction, Issues in Ad Hoc Wireless Networks

**UNIT - II**

**MAC Protocols**: Introduction, Issues in Designing a MAC protocol for Ad Hoc Wireless Networks, Design goals of a MAC Protocol for Ad Hoc Wireless Networks, Classifications of MAC Protocols, Contention - Based Protocols, Contention - Based Protocols with reservation Mechanisms, Contention – Based MAC Protocols with Scheduling Mechanisms, MAC Protocols that useDirectional Antennas, Other MAC Protocols.

**UNIT - III**

**Routing Protocols:** Introduction, Issues in Designing a Routing Protocol for Ad Hoc Wireless Networks, Classification of Routing Protocols, Table –Driven Routing Protocols, On – Demand Routing Protocols, Hybrid Routing Protocols, Routing Protocols with Efficient Flooding Mechanisms, Hierarchical Routing Protocols, Power – Aware Routing Protocols.

**UNIT - IV**

**Transport Layer Protocols:** Introduction, Issues in Designing a Transport Layer Protocol for Ad Hoc Wireless Networks, Design Goals of a Transport Layer Protocol for Ad Hoc Wireless Networks, Classification of Transport Layer Solutions, TCP Over Ad Hoc Wireless Networks, Other TransportLayer Protocol for Ad Hoc Wireless Networks.

**UNIT - V**

**Wireless Sensor Networks:** Introduction, Sensor Network Architecture, Data Dissemination, Data Gathering, MAC Protocols for Sensor Networks, Location Discovery, Quality of a Sensor Network, Evolving Standards, Other Issues.

**Textbooks:**

1. Ad Hoc Wireless Networks: Architectures and Protocols - C. Siva Ram Murthy and B. S. Manoj, 2004, PHI.
2. Wireless Ad- hoc and Sensor Networks: Protocols, Performance and Control – JagannathanSarangapani, CRC Press.

**Reference Books:**

1. Ad- Hoc Mobile Wireless Networks: Protocols & Systems, C. K. Toh, 1st Ed. Pearson Education.
2. Wireless Sensor Networks - C. S. Raghavendra, Krishna M. Sivalingam, 2004, Springer

**Sri Krishnadevaraya University College of Engineering & Technology**
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**Electronics and Communication Engineering**

| Course Code | VLSI SIGNAL PROCESSING | L | T | P | C |
|---|---|---|---|---|---|
| | Program Elective – V | 3 | 0 | 0 | 3 |
| Semester | | II | | | |

**Course Objectives:**

- To study the existing architectures suitable for VLSI.
- To understand the concepts of folding and unfolding algorithms and applications.
- To design new architectures suitable for VLSI.
- To implement fast convolution algorithms.

**Course Outcomes (CO):** Student will be able to

- Study the existing architectures suitable for VLSI.
- Understand the concepts of folding and unfolding algorithms and applications.
- Design new architectures suitable for VLSI.
- Implement fast convolution algorithms.

**UNIT - I**

**Introduction to DSP:** Typical DSP algorithms, DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction, Definitions and Properties, Solving System of Inequalities, Retiming Techniques

**UNIT - II**

**Folding and Unfolding:** Folding- Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, folding of Multirate systems Unfolding- Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding.

**UNIT - III**

**Systolic Architecture Design:** Introduction, Systolic Array Design Methodology, FIR Systolic Arrays, Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

**UNIT - IV**

**Fast Convolution:** Introduction – Cook - Toom Algorithm – Winograd algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

**UNIT - V**

**Low Power Design:** Digital lattice filter structures, bit level arithmetic, architecture, redundant arithmetic. Numerical strength reduction, synchronous, wave and asynchronous pipe lines, Scaling Vs Power Consumption, Power Analysis, Power Reduction techniques, Power Estimation Approaches

**Text books:**

1. Keshab K. Parthi, VLSI Digital Signal Processing- System Design and Implementation, WileyInter Science, 1998.
2. Kung S. Y, H. J. While House, T. Kailath ,VLSI and Modern Signal processing , Prentice Hall,1985.

**Reference Books**

1. Jose E. France, Yannis Tsividis, Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing , Prentice Hall, 1994.
2. Medisetti V. K ,VLSI Digital Signal Processing , IEEE Press (NY), 1995

**Sri Krishnadevaraya University College of Engineering & Technology**
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**Electronics and Communication Engineering**

| Course Code | IOT AND ITS APPLICATIONS<br>Program Elective – V | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| | Semester | II | | | |

**Course Objectives:**

- To apply the Knowledge in IOT Technologies and Data management.
- To determine the values chains Perspective of M2M to IOT.
- To implement the state of the Architecture of an IOT.
- To compare IOT Applications in Industrial & real world.
- To demonstrate knowledge and understand the security and ethical issues of an IOT.

**Course Outcomes (CO):** Student will be able to

- Apply the Knowledge in IOT Technologies and Data management.
- Determine the values chains Perspective of M2M to IOT.
- Implement the state of the Architecture of an IOT.
- Compare IOT Applications in Industrial & real world.
- Demonstrate knowledge and understand the security and ethical issues of an IOT.

UNIT - I

**Fundamentals of IoT:** Evolution of Internet of Things, Enabling Technologies, IoT Architectures,oneM2M, IoT World Forum (IoTWF) and Alternative IoT models, Simplified IoT Architecture and Core IoT Functional Stack, Fog, Edge and Cloud in IoT, Functional blocks of anIoT ecosystem, Sensors, Actuators, Smart Objects and Connecting Smart Objects.
IoT Platform overview: Overview of IoT supported Hardware platforms such as: Raspberry pi, ARM Cortex Processors, Arduino and Intel Galileo boards.

UNIT - II

**IoT Protocols:** IT Access Technologies: Physical and MAC layers, topology and Security of IEEE 802.15.4, 802.15.4g, 802.15.4e, 1901.2a, 802.11ah and Lora WAN, Network Layer: IP versions, Constrained Nodes and Constrained Networks, Optimizing IP for IoT: From 6LoWPAN to 6Lo, Routing over Low Power and Lossy Networks, Application Transport Methods: Supervisory Control and Data Acquisition, Application Layer Protocols: CoAP and MQTT.

UNIT - III

**Design and Development:** Design Methodology, Embedded computing logic, Microcontroller, System on Chips, IoT system building blocks, Arduino, Board details, IDE programming, Raspberry Pi, Interfaces and Raspberry Pi with Python Programming.

UNIT - IV

**Data Analytics and Supporting Services:** Structured Vs Unstructured Data and Data in Motion Vs Data in Rest, Role of Machine Learning – No SQL Databases, Hadoop Ecosystem, Apache Kafka, Apache Spark, Edge Streaming Analytics and Network Analytics, Xively Cloud for IoT, Python Web Application Framework, Django, AWS for IoT, System Management with NETCONF-YANG.

UNIT - V

**Case Studies/Industrial Applications:** IoT applications in home, infrastructures, buildings, security, Industries, Home appliances, other IoT electronic equipment's. Use of Big Data and Visualization in IoT, Industry 4.0 concepts. Sensors and sensor Node and interfacing using any Embedded target boards (Raspberry Pi / Intel Galileo/ARM Cortex/ Arduino).

**Textbooks:**

1. IoT Fundamentals: Networking Technologies, Protocols and Use Cases for Internet of Things, David Hanes, Gonzalo Salgueiro, Patrick Grossetete, Rob Barton and Jerome Henry, Cisco Press, 2017.
2. Internet of Things – A hands-on approach, ArshdeepBahga, Vijay Madisetti, Universities

| Press,2015 |
| --- |
| **Reference Books:** |
| 1. The Internet of Things – Key applications and Protocols, Olivier Hersent, David Boswarthick, Omar Elloumi and Wiley, 2012 (for Unit 2).<br>2. "From Machine-to-Machine to the Internet of Things – Introduction to a New Age of Intelligence", Jan Holler, VlasiosTsiatsis, Catherine Mulligan, Stamatis, Karnouskos, Stefan Avesand. David Boyle and Elsevier, 2014.<br>3. Architecting the Internet of Things, Dieter Uckelmann, Mark Harrison, Michahelles and Florian (Eds), Springer, 2011. |

Sri Krishnadevaraya University College of Engineering & Technology
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Electronics and Communication Engineering

# AUDIT COURSE-I

**Sri Krishnadevaraya University College of Engineering & Technology**
**Ananthapuramu-515003(A.P) India**
**Electronics and Communication Engineering**

| Course Code | ENGLISH FOR RESEARCH PAPER WRITING | L | T | P | C |
|---|---|---|---|---|---|
| | | 2 | 0 | 0 | 0 |
| Semester | | I | | | |

**Course Objectives:** This course will enable students:

- Understand the essentials of writing skills and their level of readability
- Learn about what to write in each section
- Ensure qualitative presentation with linguistic accuracy

**Course Outcomes (CO):** Student will be able to

- Understand the significance of writing skills and the level of readability
- Analyze and write title, abstract, different sections in research paper
- Develop the skills needed while writing a research paper

| UNIT - I | | 10 |
|---|---|---|

**1**Overview of a Research Paper- Planning and Preparation- Word Order- Useful Phrases - Breakingup Long Sentences-Structuring Paragraphs and Sentences-Being Concise and Removing Redundancy -Avoiding Ambiguity

| UNIT - II | | 10 |
|---|---|---|

Essential Components of a Research Paper- Abstracts- Building Hypothesis-Research Problem - Highlight Findings- Hedging and Criticizing, Paraphrasing and Plagiarism, Cauterization

| UNIT - III | | 10 |
|---|---|---|

Introducing Review of the Literature – Methodology - Analysis of the Data-Findings - Discussion-Conclusions-Recommendations.

| UNIT - IV | | 9 |
|---|---|---|

Key skills needed for writing a Title, Abstract, and Introduction

| UNIT - V | | 9 |
|---|---|---|

Appropriate language to formulate Methodology, incorporate Results, put forth Arguments and draw Conclusions

**Suggested Reading**


1. Goldbort R (2006) Writing for Science, Yale University Press (available on Google Books) Model Curriculum of Engineering & Technology PG Courses [Volume-I]
2. Day R (2006) How to Write and Publish a Scientific Paper, Cambridge University Press
3. Highman N (1998), Handbook of Writing for the Mathematical Sciences, SIAM. Highman'sbook
4. Adrian Wallwork , English for Writing Research Papers, Springer New York Dordrecht Heidelberg London, 2011

**Sri Krishnadevaraya University College of Engineering & Technology**
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**Electronics and Communication Engineering**

| Course Code | DISASTER MANAGEMENT | L | T | P | C |
|---|---|---|---|---|---|
| | | 2 | 0 | 0 | 0 |
| Semester | | I | | | |

**Course Objectives:** This course will enable students:

- Learn to demonstrate critical understanding of key concepts in disaster risk reductionand humanitarian response.
- Critically evaluate disaster risk reduction and humanitarian response policy and practice from Multiple perspectives.
- Developanunderstandingofstandardsofhumanitarianresponseandpracticalrelevanceinspecific types of disasters and conflict situations
- Criticallyunderstandthestrengthsandweaknessesofdisastermanagementapproaches, planning and programming in different countries, particularly their home country or the countries they work in

**UNIT - I**

**Introduction:** Disaster: Definition, Factors and Significance; Difference Between Hazard and Disaster;Natural and Manmade Disasters: Difference, Nature, Types and Magnitude.

**Disaster Prone Areas in India:**

Study of Seismic Zones; Areas Prone to Floods and Droughts, Landslides and Avalanches; Areas Prone to Cyclonic and Coastal Hazards with Special Reference to Tsunami; Post- Disaster Diseases and Epidemics

**UNIT - II**

**Repercussions of Disasters and Hazards**:

Economic Damage, Loss of Human and Animal Life, Destruction of Ecosystem. Natural Disasters: Earthquakes, Volcanisms, Cyclones,Tsunamis,Floods,DroughtsandFamines,Landslides and Avalanches, Man-made disaster: Nuclear Reactor Meltdown, Industrial Accidents, Oil Slicks and Spills, Outbreaks of Disease and Epidemics, War and Conflicts.

**UNIT - III**

**Disaster Preparedness and Management:**

Preparedness: Monitoring of Phenomena Triggering Disaster Hazard; Evaluation of Risk: Application of Remote Sensing, Data from Meteorological and Other Agencies, Media Reports: Governmental and Community Preparedness.

**UNIT - IV**

**Risk Assessment Disaster Risk:**

Concept and Elements, Disaster Risk Reduction, Global and National Disaster Risk Situation. Techniques of Risk Assessment, Global Co-Operation in Risk Assessment and Warning, People's Participationin Risk Assessment. Strategies for Survival.

**UNIT - V**

**Disaster Mitigation:** Meaning, Concept and Strategies of Disaster Mitigation, Emerging Trends in Mitigation. Structural Mitigation and Non-Structural Mitigation, Programs of Disaster Mitigation in India.

**Suggested Reading**

1. R.Nishith,SinghAK,"DisasterManagementinIndia:Perspectives,issuesandstrategies
2. "'New Royal book

Company..Sahni,PardeepEt.Al.(Eds.),"DisasterMitigationExperiencesAndReflections",PrenticeHall OfIndia, New Delhi.
3. GoelS.L., Disaster Administration And Management Text and Case Studies",Deep & Deep Publication Pvt. Ltd., New Delhi

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**Electronics and Communication Engineering**

| Course Code | SANSKRITFOR TECHNICAL KNOWLEDGE | L | T | P | C |
|---|---|---|---|---|---|
| | | 2 | 0 | 0 | 0 |
| **Semester** | | **I** | | | |

**Course Objectives:** This course will enable students:

- To get a working knowledge in illustrious Sanskrit, the scientific language in the world
- Learning of Sanskrit to improve brain functioning
- Learning of Sanskrit to develop the logic in mathematics, science &other subjects enhancing the memory power
- The engineering scholars equipped with Sanskrit will be able to explore the huge
- Knowledge from ancient literature

**Course Outcomes (CO):** Student will be able to

- Understanding basic Sanskrit language
- Ancient Sanskrit literature about science &technology can be understood
- Being a logical language will help to develop logic in students

**UNIT - I**

Alphabets in Sanskrit,

**UNIT - II**

Past/Present/Future Tense, Simple Sentences

**UNIT - III**

Order, Introduction of roots

**UNIT - IV**

Technical information about Sanskrit Literature

**UNIT - V**

Technical concepts of Engineering-Electrical, Mechanical, Architecture, Mathematics

**Suggested Reading**

1.“Abhyaspustakam” –Dr.Vishwas, Sanskrit-Bharti Publication, New Delhi
2.“Teach Yourself Sanskrit” Prathama Deeksha- VempatiKutumbshastri, RashtriyaSanskrit Sansthanam, New Delhi Publication
3.“India’s Glorious ScientificTradition” Suresh Soni, Ocean books (P) Ltd.,New Delhi



# AUDIT COURSE-II

**Sri Krishnadevaraya University College of Engineering & Technology**
**Ananthapuramu-515003(A.P) India**
**Electronics and Communication Engineering**

| Course Code | PEDAGOGY STUDIES | L | T | P | C |
|---|---|---|---|---|---|
| | | 2 | 0 | 0 | 0 |
| Semester | | II | | | |

**Course Objectives:** This course will enable students:

- Review existing evidence on their view topic to inform programme design and policy making undertaken by the DfID, other agencies and researchers.
- Identify critical evidence gaps to guide the development.

**Course Outcomes (CO):** Student will be able to

Students will be able to understand:

- What pedagogical practices are being used by teachers informal and informal classrooms in developing countries?
- What is the evidence on the effectiveness of these pedagogical practices, in whatconditions, and with what population of learners?
- Howcanteachereducation(curriculumandpracticum)andtheschoolcurriculumand guidancematerials best support effective pedagogy?

**UNIT - I**

**Introduction and Methodology:** Aims and rationale, Policy background, Conceptual frame work and terminology Theories of learning, Curriculum, Teacher education. Conceptual framework, Research questions**.** Overview of methodology and searching.

**UNIT - II**

**Thematic overview:** Pedagogical practices are being used by teachers in formal and informal classrooms in developing countries. Curriculum, Teacher education.

**UNIT - III**

Evidence on the effectiveness of pedagogical practices, Methodology for the in-depth stage: quality assessment of included studies. How can teacher education (curriculum and practicum) and the school curriculum and guidance materials best support effective pedagogy? Theory of change. Strength and nature of the body ofevidence for effective pedagogical practices. Pedagogic theory and pedagogical approaches. Teachers' attitudes and beliefs and Pedagogic strategies.

**UNIT - I**V

**Professional development:** alignment with classroom practices and follow-up support, Peer support, Support from the head teacher and the community. Curriculum and assessment, Barriers to learning limited resources and large class
sizes

**UNIT - V**

**Research gaps and future directions:** Research design**,** Contexts**,** Pedagogy**,** Teacher education**,** Curriculum and assessment**,** Dissemination and research impact.

**Suggested Reading**


1. AckersJ,HardmanF(2001)ClassroominteractioninKenyanprimaryschools,Compare, 31 (2): 245-261.
2. AgrawalM(2004)Curricularreforminschools:Theimportanceofevaluation,Journalof
3. Curriculum Studies, 36 (3): 361-379.

4. AkyeampongK(2003) Teacher training in Ghana - does it count? Multi-site teacher educationresearch project (MUSTER) country report 1. London: DFID.
5. Akyeampong K, LussierK, PryorJ, Westbrook J (2013) Improving teaching and learning of basicmaths and reading in Africa: Does teacher preparation count? International Journal Educational Development, 33 (3): 272–282.
6. Alexander RJ(2001) Culture and pedagogy: International comparisons in primary education. Oxford and Boston: Blackwell.
Chavan M (2003)Read India: A mass scale, rapid, 'learning to read' campaign.
7. www.pratham.org/images/resource%20working%20paper%202.pdf.

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**Electronics and Communication Engineering**

| Course Code | STRESSMANAGEMENT BY YOGA | L | T | P | C |
|---|---|---|---|---|---|
| | | 2 | 0 | 0 | 0 |
| Semester | | II | | | |

**Course Objectives:** This course will enable students:

- To achieve overall health of body and mind
- To overcome stress

**Course Outcomes (CO):** Student will be able to

- Develop healthy mind in a healthy body thus improving social health also
- Improve efficiency

| | | |
|---|---|---|
| **UNIT - I** | | |
| Definitions of Eight parts of yog. (Ashtanga) | | |
| **UNIT - II** | | |
| Yam and Niyam. | | |
| **UNIT - III** | | |
| Do`s and Don't'sin life.<br>i) Ahinsa,satya,astheya,bramhacharyaand aparigrahaii)Shaucha,santosh,tapa,swadhyay,ishwarpranidhan | | |
| **UNIT - I**V | | |
| Asan and Pranayam | | |
| **UNIT - V** | | |
| i)Various yoga poses and their benefits formind & body ii) Regularization of breathing techniques and its effects-Types of pranayam | | |

**Suggested Reading**

1. 'Yogic Asanas for Group Tarining-Part-I": Janardan Swami Yogabhyasi Mandal, Nagpur
2. "Rajayogaor conquering the Internal Nature" by Swami Vivekananda, AdvaitaAshrama (Publication Department), Kolkata

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**Electronics and Communication Engineering**

| Course Code | PERSONALITY DEVELOPMENT THROUGH LIFE ENLIGHTENMENT SKILLS | L | T | P | C |
|---|---|---|---|---|---|
| | | 2 | 0 | 0 | 0 |
| Semester | | II | | | |

**Course Objectives:** This course will enable students:

- To learn to achieve the highest goal happily
- To become a person with stable mind, pleasing personality and determination
- To awaken wisdom in students

**Course Outcomes (CO):** Student will be able to

- StudyofShrimad-Bhagwad-Geetawillhelpthestudentindevelopinghispersonalityand achievethe highest goal in life
- The person who has studied Geeta will lead the nation and mankind to peace and prosperity
- Study of Neeti shatakam will help in developing versatile personality of students

**UNIT - I**

Neetisatakam- Holistic development of personalityVerses-19,20,21,22(wisdom)
Verses-29,31,32(pride &heroism)
Verses-26,28,63,65(virtue)

**UNIT - II**

Neetisatakam- Holistic development of personalityVerses-52,53,59(dont's)
Verses-71,73,75,78(do's)

**UNIT - III**

Approach to day-to-day work and duties.
Shrimad Bhagwad Geeta: Chapter2-Verses41,47,48, Chapter3-Verses13,21,27,35,Chapter6-Verses5,13,17,23,35,Chapter18-Verses45,46,48.

**UNIT - IV**

Statements of basic knowledge.
Shrimad Bhagwad Geeta: Chapter2-Verses 56,62,68Chapter12 -Verses13,14,15,16,17,18
Personality of Role model. Shrimad Bhagwad Geeta:

**UNIT - V**

Chapter2-Verses 17, Chapter3-Verses36,37,42,Chapter4-Verses18,38,39
Chapter18– Verses37,38,63

**Suggested Reading**

1. "Srimad Bhagavad Gita" by Swami Swarupananda Advaita Ashram (PublicationDepartment), Kolkata
2. Bhartrihari'sThree Satakam (Niti-sringar-vairagya) by P.Gopinath, RashtriyaSanskritSansthanam, New Delhi.



# OPEN ELECTIVE

**Sri Krishnadevaraya University College of Engineering & Technology**
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**Electronics and Communication Engineering**

| Course Code | INDUSTRIAL SAFETY | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| | Semester | III | | | |

**Course Objectives:**

- To know about Industrial safety programs and toxicology, Industrial laws, regulations and source models
- To understand about fire and explosion, preventive methods, relief and its sizing methods
- To analyze industrial hazards and its risk assessment.

**Course Outcomes (CO):** Student will be able to

- To list out important legislations related to health, Safety and Environment.
- To list out requirements mentioned in factories act for the prevention of accidents.
- To understand the health and welfare provisions given in factories act.

**UNIT - I**

Industrial safety: Accident, causes, types, results and control, mechanical and electrical hazards, types, causes and preventive steps/procedure, describe salient points of factories act 1948 for health and safety, wash rooms, drinking water layouts, light, cleanliness, fire, guarding, pressure vessels, etc, Safety color codes. Fire prevention and firefighting, equipment and methods.

**UNIT - II**

Fundamentals of maintenance engineering: Definition and aim of maintenance engineering, Primary and secondary functions and responsibility of maintenance department, Types of maintenance, Types and applications of tools used for maintenance, Maintenance cost & its relationship with replacement economy,Service life of equipment.

**UNIT - III**

Wear and Corrosion and their prevention: Wear- types, causes, effects, wear reduction methods, lubricants-types and applications, Lubrication methods, general sketch, working and applications, i. Screw down grease cup, ii. Pressure grease gun, iii. Splash lubrication, iv. Gravity lubrication, v. Wick feed lubrication vi. Side feed lubrication, vii. Ring lubrication, Definition, principle and factors affecting the corrosion. Types of corrosion, corrosion prevention methods.

**UNIT - IV**

Fault tracing: Fault tracing-concept and importance, decision tree concept, need and applications, sequence of fault finding activities, show as decision tree, draw decision tree for problems in machine tools, hydraulic, pneumatic, automotive, thermal and electrical equipment's like, I. Any one machine tool, ii. Pump iii. Air compressor, iv. Internal combustion engine, v. Boiler, vi. Electrical motors, Types of faults in machine tools and their general causes.

**UNIT - V**

Periodic and preventive maintenance: Periodic inspection-concept and need, degreasing, cleaning and repairing schemes, overhauling of mechanical components, overhauling of electrical motor, common troubles and remedies of electric motor, repair complexities and its use, definition, need, steps and advantages of preventive maintenance. Steps/procedure for periodic and preventive maintenance of: I. Machine tools, ii. Pumps, iii. Air compressors, iv. Diesel generating (DG) sets, Program and schedule of preventive maintenance of mechanical and electrical equipment, advantages of preventive maintenance. Repair cycle concept and importance

**Textbooks:**

1. Maintenance Engineering Handbook, Higgins & Morrow, Da Information Services.
2. Maintenance Engineering, H. P. Garg, S. Chand and Company.

**Reference Books:**

1. Pump-hydraulic Compressors, Audels, Mcgrew Hill Publication.
2. Foundation Engineering Handbook, Winterkorn, Hans, Chapman & Hall London.

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**Electronics and Communication Engineering**

| Course Code | BUSINESS ANALYTICS | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| | Semester | III | | | |

**Course Objectives:**

- The main objective of this course is to give the student a comprehensive understanding ofbusiness analytics methods.

**Course Outcomes (CO):** Student will be able to

- Students will demonstrate knowledge of data analytics.
- Students will demonstrate the ability of think critically in making decisions based ondata and deep analytics.
- Students will demonstrate the ability to use technical skills in predicative andprescriptive modeling to support business decision-making.
- Students will demonstrate the ability to translate data into clear, actionable insights.

**UNIT - I**

Business Analysis: Overview of Business Analysis, Overview of Requirements, Role of the Business Analyst.
Stakeholders: the project team, management, and the front line, Handling Stakeholder Conflicts.

**UNIT - II**

Life Cycles: Systems Development Life Cycles, Project Life Cycles, Product Life Cycles, Requirement Life Cycles.

**UNIT - III**

Forming Requirements: Overview of Requirements, Attributes of Good Requirements, Types of Requirements, Requirement Sources, Gathering Requirements from Stakeholders, Common Requirements Documents. Transforming Requirements: Stakeholder Needs Analysis, Decomposition Analysis, Additive/Subtractive Analysis, Gap Analysis, Notations (UML & BPMN), Flowcharts, Swim Lane Flowcharts, Entity-Relationship Diagrams, State-Transition Diagrams, Data Flow Diagrams, Use Case Modeling, Business Process Modeling

**UNIT - IV**

Finalizing Requirements: Presenting Requirements, Socializing Requirements and Gaining Acceptance, Prioritizing Requirements. Managing Requirements Assets: Change Control, Requirements Tools

**UNIT - V**

Recent Trands in: Embedded and colleborative business intelligence, Visual data recovery, Data Storytelling and Data Journalism.

**Textbooks:**

1. Business Analysis by James Cadle et al.
2. Project Management: The Managerial Process by Erik Larson and, Clifford Gray

**Reference Books:**

1. Business analytics Principles, Concepts, and Applications by Marc J. Schniederjans, Dara G. Schniederjans, Christopher M. Starkey, Pearson FT Press.
2. Business Analytics by James Evans, persons Education.

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**Electronics and Communication Engineering**

| Course Code | WASTE TO ENERGY | L | T | P | C |
|---|---|---|---|---|---|
| | | 3 | 0 | 0 | 3 |
| Semester | | III | | | |

**Course Objectives:**

- Introduce and explain energy from waste, classification and devices to convert waste toenergy.
- To impart knowledge on biomass pyrolysis, gasification, combustion and conversion process.
- To educate on biogas properties, bio energy system, biomass resources and their classification and biomass energy programme in India.

**Course Outcomes (CO):** Student will be able to

- To know about overview of Energy to waste and classification of waste.
- To acquire knowledge on biomass pyrolysis, gasification, combustion and conversion processin detail.
- To gain knowledge on properties of biogas, biomass resources and programmes to convert waste to energy in India.

**UNIT - I**

Introduction to Energy from Waste: Classification of waste as fuel – Agro based, Forest residue, Industrial waste - MSW – Conversion devices – Incinerators, gasifiers, digestors

**UNIT - II**

Biomass Pyrolysis: Pyrolysis – Types, slow fast – Manufacture of charcoal – Methods - Yields and application – Manufacture of pyrolytic oils and gases, yields and applications.

**UNIT - III**

Biomass Gasification: Gasifiers – Fixed bed system – Downdraft and updraft gasifiers – Fluidized bed gasifiers – Design, construction and operation – Gasifier burner arrangement for thermal heating – Gasifier engine arrangement and electrical power – Equilibrium and kinetic considerationin gasifier operation

**UNIT - IV**

Biomass Combustion: Biomass stoves – Improved chullahs, types, some exotic designs, Fixed bed combustors, Types, inclined grate combustors, Fluidized bed combustors, Design, construction and operation - Operation of all the above biomass combustors.

**UNIT - V**

Biogas: Properties of biogas (Calorific value and composition) - Biogas plant technology and status - Bio energy system - Design and constructional features - Biomass resources and their classification - Biomass conversion processes - Thermo chemical conversion - Direct combustion - biomass gasification- pyrolysis and liquefaction - biochemical conversion - anaerobic digestion - Types of biogas Plants – Applications - Alcohol production from biomass - Bio diesel production -
Urban waste to energy conversion - Biomass energy programme in India.

**Textbooks:**

1. Non-Conventional Energy, Desai, Ashok V., Wiley Eastern Ltd., 2018
2. Biogas Technology - A Practical Hand Book - Khandelwal, K. C. and Mahdi, S. S., TMH, 2017

**Reference Books:**

1. Food, Feed and Fuel from Biomass, Challal, D. S., IBH Publishing Co. Pvt. Ltd., 1991.
2. Biomass Conversion and Technology, C. Y. WereKo-Brobby and E. B. Hagan, John Wiley