SRI KRISHNADEVARAYA UNIVERSITY

COLLEGE OF ENGINEERING AND TECHNOLOGY: ANANTAPURAM

ACADEMIC REGULATIONS 2013 FOR M.Tech (Regular) DEGREE COURSE

(Effective for the students admitted into first year from the academic year 2013-2014)

The M.Tech Degree of Sri Krishnadevaraya University College of Engineering and Technology Anantapuram shall be conferred on candidates who are admitted to the program and fulfill all the requirements for the award of the Degree.

1.0 Courses of Study

1.1 The following specializations are offered at present for the M.Tech course of study.

S.No.	Department	Specialization
1	Computer Science and Engineering	Computer Science and Engineering
2	Electronics and Communications Engineering	Embedded Systems and VLSI Design
3	Electrical and Electronics Engineering	Electrical Power Systems

2.0 Eligibility for Admissions

2.1 Admission to the above program shall be made subject to the eligibility, qualifications and specialization prescribed by the University from time to time.

2.2 Admissions shall be made on the basis of merit rank obtained by the qualifying candidate in GATE or PGECET or on the basis of any other order of merit approved by the University, subject to reservations prescribed by the university from time to time.

3.0 Award of Degree

3.1 A student shall be declared eligible for the award of the M.Tech degree, if he/she pursues a course of study and completes it successfully for not less than two academic years (Four Semesters) and not more than four academic years.

3.2 A student, who fails to fulfill all the academic requirements for the award of the degree within four academic years from the year of his/her admission, shall forfeit his/her seat in M.Tech course.

4.0 Attendance

4.1 The minimum instruction for each semester is 90 days.

4.2 A candidate shall be deemed to have eligible to write End Semester University examinations if he/she has put in a minimum of 75% of attendance in aggregate of all the subjects.

4.3 Condonation of shortage of attendance up to 10% i.e. 65% and above, and below 75% may be given by the College academic committee.

4.4 Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representations by the candidate with supporting evidence to the college principal.

4.5 A candidate shall not be promoted to the next semester unless he/she fulfills the attendance requirements of the previous semester.

4.6 A stipulated fee shall be payable towards condonation of shortage of attendance.

5.0Evaluation

5.1 The performance of the candidate in each semester shall be evaluated subject-wise, with a maximum of 100 marks for theory subject and 100 marks for Laboratory, on the basis of Internal Evaluation and End Semester University Examination.

5.2 For theory subjects 60 marks shall be awarded based on the performance in the End Semester University Examination and 40 marks shall be awarded based on the Internal Evaluation. The internal evaluation shall be based on two midterm examinations. First midterm examination shall be conducted for the first half of the syllabus in the middle of the semester and second midterm examination shall be conducted for the second half of the syllabus towards the end of the semester. A weightage of 0.75 for better score and 0.25 for the other score will be considered for awarding the sessional marks in both the midterm examinations. Each midterm examination shall be conducted for duration of 120 minutes with 4 questions to be answered out of 4 questions.

5.3 For practical subjects 50 marks shall be awarded based on the performance in the End Semester Examinations, 50 marks shall be awarded based on the performance in Laboratory as Internal assessment.

5.4 Laboratory examination for M.Tech courses must be conducted with two Examiners, one of them being Laboratory Class Teacher and second examiner shall be appointed by the Principal from the panel of examiners submitted by the Head of the Department.

5.5 A candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Semester University Examination and a minimum aggregate of 50% of the total marks in the End Semester University Examination and Internal Evaluation taken together.

5.6 In case the candidate does not secure the minimum academic requirement in any subject he has to reappear for the End Semester University Examination in that subject.

5.7 There shall be a seminar presentation at the end of 3rd semester. For seminar, a student under the supervision of a faculty member, shall collect the literature on a relevant topic and critically review the literature and submit it to the Department in a report form and shall make an oral presentation before the Departmental Committee. The Departmental Committee consists of Head of the Department, supervisor and two other senior faculty members of the department. For Seminar there will be only internal evaluation of 100 marks. A candidate has to secure a minimum of 50% to be declared successful.

6.0Evaluation of Project Work/Dissertation

6.1 The work on the project shall be initiated in the beginning of 3rd semester and the duration of the project is for 3rd and 4th semesters.

6.2 A candidate is permitted to register for the Project Work after satisfying the attendance requirement of all the subjects (theory and practical) of 1st and 2nd semesters.

6.3 A Project Review Committee (PRC) shall be constituted with Principal/his nominee as chair person, Head of the Department and one other senior faculty member of the concerned department apart from the guide. The concerned Head of the Department will be the convener for all the PRC meetings.

6.4 A candidate has to submit, in consultation with his project supervisor, the title, objective and plan of action of his project work (Based on a publication in a peer Reviewed Journal) to the Project Review Committee for its approval before the second semester end examinations. After obtaining the approval of the PRC the student can initiate the Project work after the second semester end examinations.

6.5 Every candidate shall work on projects approved by the PRC of the college.

6.6 If a candidate wishes to change his supervisor or topic of the project he can do so with approval of the PRC. However, the PRC shall examine whether the change of topic/supervisor leads to a major

change of his initial plans of project proposal. If so, his date of registration for the project work starts from the date of change of Supervisor or topic as the case may be.

6.7 A candidate shall submit status report in two stages at least with a gap of 3 months between them.

6.8 A candidate shall be allowed to submit the project report only after fulfilling the attendance requirements of all the semesters with the approval of PRC and not earlier than 40 weeks from the date of registration of the project work. For the approval of PRC the candidate shall submit the draft copy of thesis to the Head of the Department and shall make an oral presentation before the PRC.

6.9 The Candidate is desired to publish the work/accepted to be published in a journal or presented in a national/international conference/seminar of repute and relevance in order to submit the Project Report /dissertation.

6.10 Three copies of the dissertation/Project Report certified by the supervisor and the concerned Head of the Department in the prescribed form shall be submitted to the College. Once a student fails to submit the dissertation within the stipulated period of four semesters, extension of time up to one more year may be permitted by the Principal with recommendation of the College Academic Council. Beyond this period, extension may be given with the permission of the university by collecting the prescribed fee.

6.11 The dissertation shall be adjudicated by an external examiner nominated by the Vice Chancellor from among the panel of examiners submitted by the Principal in consultation with the concerned Head of the Department.

6.12 The Viva voce examination shall be conducted at the end of 3rd semester (Project work Part-A) and at the end of 4th semester or later depending on the completion of the project

6.13 The viva-voce examination shall be conducted by a board consisting of the supervisor, Head of the Department and the examiner who adjudicated the Dissertation.

The Board shall jointly report candidates work as:

A. Excellent

B. Good

C. Satisfactory

D. Unsatisfactory

Head of the Department shall coordinate and make arrangements for the conduct of viva-voce examination. If the report of the viva-voce is unsatisfactory, the candidate will retake the viva-voce examination within six months. If he fails to get a satisfactory report at the second viva-voce examination, the candidate may be asked to submit a new project proposal to PRC.

7.0Award of Class

7.1 After a student has satisfied the requirements prescribed for the completion of the course and is eligible for the award of M. Tech. Degree he shall be placed in one of the following three classes:

Class Awarded	**% of marks to be secured**
First Class with Distinction	75% and above(Without any Supplementary Appearance) and 'A' grade in project
First Class	Below 75% but not less than 60% and A or B or C grade in Project
	75% and above (With Supplementary Appearance) and A or B or C grade in Project
Second Class	Below 60% but not less than 50% and A or B or C grade in Project

(The marks in internal evaluation and end semester University examination shall be shown separately in the marks memorandum and also the project grade)

8.0General

8.1 The academic regulations should be read as a whole for purpose of any interpretation.

8.2 In case of any doubt or ambiguity in the interpretation of the above rules, the decision of the University is final.

8.3 The University may change or amend the academic regulations and syllabus at any time and the changes and amendments made shall be applicable to all the students with effect from the date notified by the University.

Sri Krishnadevaraya University College of Engineering and Technology : Anantapur
Department of Electronics and Communications Engineering

M.Tech I Year I Semester Course Structure

S.No.	Abbreviation	Subject	Periods / Week		C	Marks		
			L	T/P		Internal	External	Total
1.	MCI	Microcontrollers and Interfacing	4	-	4	40	60	100
2.	ESC	Embedded System Concepts & Design	4	-	4	40	60	100
3.	VTD	VLSI Technology and Design	4	-	4	40	60	100
4.	DSD	Digital System Design	4	-	4	40	60	100
5.	CFA	CPLD/FPGA Architectures & Applications	4	-	4	40	60	100
6.	MIL	Microcontrollers and Interfacing Lab	-	4	2	40	60	100
7.	CFL	CPLD/FPGA Lab	-	4	2	40	60	100
		TOTAL	20	8	24	280	420	700

M.Tech I Year II Semester Course Structure

S.No.	Abbreviation	Subject	Periods / Week		C	Marks		
			L	T/P		Internal	External	Total
1.	RTS	Real Time Operating Systems	4	-	4	40	60	100
2.	VPD	VLSI Physical Design Automation	4	-	4	40	60	100
3.	CID	CMOS Digital IC Design	4	-	4	40	60	100
4.	E-I	Elective-I 1. Low Power VLSI Design 2. Hardware Software Core Design 3. Device Modelling	4	-	4	40	60	100
5.	E-II	Elective-II 1. Advanced DSP and Applications 2. Network Security and Cryptography 3. MEMS	4	-	4	40	60	100
6.	EPL	Embedded Systems Programming Lab	-	4	2	40	60	100
7.	CIL	CMOS Digital IC Design Lab	-	4	2	40	60	100
		TOTAL	20	8	24	280	420	700

L – Lecture, T – Tutorial, P - Practical

M.Tech II Year I Semester Course Structure

SUBJECTS	CREDITS	MAX.MARKS		TOTAL	Min.Marks/grades to pass
	C	Int.	Ext.		
Seminar	6	100	-	100	50
Project Part - A	8	-	-	-	-

M.Tech II Year II Semester Course Structure

SUBJECTS	CREDITS	MAX.MARKS		TOTAL	Min.Marks/grades to pass
	C	Int.	Ext.		
Project Part B Grades:A,B,C,D A- Excellent B- Good C- Satisfactory D- Unsatisfactory	18	-	-	-	A/B/C

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SR57101 – MICRO CONTROLLERS & INTERFACING

UNIT I

INTEL 8051: Architecture of 8051, Memory Organization, Register banks, Bit addressing media, SFR area, addressing modes, Instruction set, Programming examples.

UNIT II

8051 Interrupt structure, Timer modules, Serial Features, Port structure, Power saving modes.

UNIT III

MOTOROLA 68HC11: Controllers features, Different modes of operation and memory map, Functions of I/O ports in single chip and expanded multiplexed mode, Timer system.

UNIT IV

Input capture, Output compare and pulsed accumulator features of 68HC11, Serial peripherals, Serial Communication interface, Analog to digital conversion features.

UNIT V

PIC MICROCONTROLLERS: Program memory, CPU registers, Register file structure, Block diagram of PIC 16C74, I/O ports. Timer 0,1 and 2 features, Interrupt logic, serial peripheral interface, PIC family parts, I2C.

UNIT VI

MICROCONTROLLER INTERFACING: 8051, 68HC11, PIC-16C6X and External Memory Interfacing, On Chip Counters, Timers, Serial I/O, Interrupts and their use. UART,RTC,ADC,PWM, Watch dog, ISP, IAP features.

TEXT BOOKS:

1) M.A. Mazadi, J.G. Mazidi & Rolin D.McKinlay "The 8051 Micro Controller & Embedded Systems using assembly and C", Pearson Education. Asia, 2nd edition, 2006.
2) John B. Peatman, Designing with PIC Micro Controllers, Low price edition, Pearson Education, 7th reprint 2004.
3) Jonathan W. Valvano, Embedded Microcomputer systems, Real Time Interfacing, Brookes/Cole, Thomas learning, 2nd edition 2007.

REFERENCES:

1) 8-bit Embedded Controllers, INTEL Corporation 1990.
2) Motorola 68HC11 data sheets.
3) PIC 16C74 data sheets.

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SR57102 – EMBEDDED SYSTEM CONCEPTS & DESIGN

UNIT I

INTRODUCTION: Embedded system overview, embedded hardware units, embedded software in a system, embedded system on chip (SOC), design process, classification of embedded systems.

UNIT II

EMBEDDED COMPUTING PLATFORM: CPU Bus, memory devices, component interfacing, networks for embedded systems, communication interfacings: RS232/UART, RS422/RS485, IEEE 488 bus.

UNIT III

SURVEY OF SOFTWARE ARCHITECTURE: Round robin, round robin with interrupts, function queue scheduling architecture, selecting an architecture saving memory space.

UNIT IV

EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and target machines, linkers, locations for embedded software, getting embedded software into target system, debugging technique.

UNIT V

RTOS CONCEPTS: Architecture of the kernel, interrupt service routines, semaphores, message queues, pipes.

UNIT VI

INSTRUCTION SETS: Introduction, preliminaries, ARM processor, SHARC processor.

TEXT BOOKS:

1) Computers as a component: principles of embedded computing system design- wayne wolf, reprint 2009.
2) An embedded software premier: David E. Simon, 2007, 4th edition.
3) Embedded/real time systems-KVKK Prasad, Dreamtech press, 2005

REFERENCES:

1) Embedded real time systems programming-Sri ram V Iyer, Pankaj Gupta, TMH, 2004.
2) Embedded system design- A unified hardware/software introduction- frank vahid, tony D. Givargis, John Willey, 2002.

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SR57103 – VLSI TECHNOLOGY AND DESIGN

UNIT I

INTRODUCTION TO MOS TECHNOLOGY: Overview of VLSI Design Methodologies**,** VLSI Design flow, Styles of VLSI Design, CAD Technology, MOS Transistors and its Trends.

BASIC ELECTRICAL PROPERTIES OF MOS: Ids-Vds Relationships, Threshold voltage Vt, gm, gds and Wo, Pass Transistor, MOS Zpu/Zpd, MOS Transistor circuit model.

UNIT II

CMOS Design: CMOS Logic, CMOS Gate Design, Transmission Gate Logic Design, Bi-CMOS Inverters, Latch-up in CMOS circuits.

UNIT III

LAYOUT DESIGN AND TOOLS: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

UNIT IV

LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNIT V

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network Delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

UNIT VI

SEQUENTIAL SYSTEMS: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

TEXT BOOKS:

1. K. Eshraghian etal.(3 authors), “Essentials of VLSI Circuits and Systems”, PHI of India Ltd.,
2. Wayne Wolf, “Modern VLSI Design”, 3/E, Pearson Education, fifth Indian Reprint, 2005.
3. Sung-Mo Kang and Yusuf Leblebici, “CMOS Digital Integrated Circuits Analysis and Design” TATA McGraw Hill, 3rd Edition, 2003.

REFERENCES:

1. N.H.E Weste, K.Eshraghian, “Principals of CMOS Design”, Addison Wesley, 2nd Edition.
2. Ken Martin, “Digital Integrated Circuits Design” oxford University Press, 2nd impression, 2005.

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SR57104 – DIGITAL SYSTEM DESIGN

UNIT I

DESIGN OF DIGITAL SYSTEMS: ASM charts, Hardware description language and control sequence method, Reduction of state tables, state assignments.

UNIT II

SEQUENTIAL CIRCUIT DESIGN: design of Iterative circuits, design of sequential circuits using ROMs and PLAs, sequential circuit design using CPLD, FPGAs.

UNIT III

FAULT MODELING: Fault classes and models, stuck at faults, bridging faults, transition and intermittent faults.

TEST GENERATION: Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm.

UNIT IV

TEST PATTERN GENERATION: D–algorithm, PODEM, Random testing, transition count testing, Signature analysis and testing for bridging faults.

UNIT V

FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS: State identification and fault detection experiment. Machine identification, Design of fault detection experiment.

UNIT VI

PROGRAMMING LOGIC ARRAYS: Design using PLAs, PLA minimization and PLA folding.

PLA TESTING: Fault models, Test generation and Testable PLA design.

TEXTBOOKS:

1. Kohavi – “Switching & finite Automata Theory” (TMH), 2nd edition.
2. N. Biswas – “Logic Design Theory” (PHI), 2006.
3. Olman Balabanian, Bradley Calson – “Digital Logic Design Principles” – Wily Student Edition 2004.

REFRENCES:

1. M.Abramovici, M.A.Breues, A.D. Friedman – “Digital System Testing and Testable Design”, Jaico Publications, 2008.
2. Charles H. Roth Jr. – “Fundamentals of Logic Design”, 5th edition, 2005, Singapore Publications.
3. Frederick. J. Hill & Peterson – “Computer Aided Logic Design” – John Wiley & Son‟s publications, 4th Edition, 1993.

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SR57105 – CPLD & FPGA ARCHITECTURE & APPLICATIONS

UNIT I

PROGRAMMABLE LOGIC: ROM, PLA, PAL, PLD, FPGA – Features, Complex Programmable Logic Devices: ALTERA CPLDs and ALTERA FLEX 10k Series CPLD, Speed Performance.

UNIT II

FPGA: Xilinx logic Cell array, CLB,I/O Block Programmable interconnect, Technology Mapping for FPGA: Library based, LUT based, Multiplexer based Technology Mapping.

UNIT III

CASE STUDIES: programming Technologies, Xilinx XC3000, XC4000, Actel FPGAs, Alteras FPGAs, Plus Logic FPGA, AMD FPGA, Quick Logic FPGA, Algotronix FPGA, Cross point solutions FPGA, FPGA Design Flow.

UNIT IV

FINITE STATE MACHINES (FSM): Finite State Machine– State Transition Table, State Assignments for FPGAs. Problem of the Initial State Assignment for One Hot Encoding.

UNIT V

REALIZATION OF STATE MACHINE: Derivation of SM Charts. Realization of State Machine Chart, Alternative Realization of State Machine Chart using Microprogramming. Linked State Machines. One–Hot State Machine, Petri nets for State Machines – Basic Concepts, Properties. Extended Petri nets for Parallel Controllers.

UNIT VI

FSM ARCHITECTURES: Architectures Centered Around Non-Registered PLDs. State Machine Designs Centered Around A Shift Register.

SYSTEMS LEVEL DESIGN: One–Hot Design Method. Use of ASMs in One–Hot Design. Application of One–Hot Method. System Level Design: Controller, Data Path and Functional Partition.

TEXT BOOKS:

1. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall (Pte), 1994.
2. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.

REFERENCES:

1. Fundamentals of logic Design, 5/e, Charles H Roth.Jr.
2. S. Brown, R. Francis, J. Rose, Z. Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.
3. Engineering Digital Design, 2/e, Richard F Tinder **Unit VI & VII**..

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REAL TIME OPERATING SYSTEMS

UNIT-I

REAL TIME OPERATING SYSTEMS: Architecture of kernel, Tasks and Task scheduler, interrupt services routines, semaphores, mutex, mailboxes, message queues, event register, pipes, signals, timers, memory management, priority inversion problem.

UNIT-II

REAL TIME APPLICATIONS: Digital control, High level controls, signal processing, other real time applications.

UNIT-III

HARD VERSUS SOFT REAL TIME SYSTEMS: Jobs and processors, release times, deadlines, and timing constraints. Hard and soft timing constraints. Hard real time systems, soft real time systems.

UNIT-IV

REAL TIME SCHEDULING APPROACHES: Clock Driven, Weighted round robin, priority driven, dynamic vs static systems, effective release times an dead lines.

UNIT-V

REAL TIME OPERATING SYSTEM: QNX Neutrino, VX works, Microc/os-II, RT Linux ,overview of unix/Linux.

UNIT-VI

SHELL AND SYSEM PROGRAMMING: Shell programming-shell variables, shell programming constructs, processes, signals, multithreading, semaphores, mutex, shared memory, messagequeue.

TEXTBOOKS

1) Embedded Real Time Systems-Blackbook Dr.K.V.K.K.Prasad, 2005 edition, Dreamtech press.
2) Jane W.S.Liu,"Real Time Systems",Pearson education, 2007.
3) C.M.Krishna,KANG G.Shin,"Real Time Systems",McGraw Hill, 1997.

REFERENCES

1) www.kernel.org.
2) Vxworks Programming Guide.

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VLSI PHYSICAL DESIGN AUTOMATION

UNIT I

PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT II

Layout Compaction, Placement, Floor planning And Routing Problems, Concepts and Algorithms.

UNIT III

MODELLING AND SIMULATION: Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT IV

LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis.

UNIT V

HIGH-LEVEL SYNTHESIS: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT VI

PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA technologies, Physical Design cycle for FPGA"s, partitioning and routing for segmented and staggered Models.

TEXTBOOKS:

1) S.H.Gerez, "Algorithms for VLSI Design Automation", Wiley Student Edition, John Wiley & Sons (Asia) Pvt. Ltd., 1999.

2) Naveed Sherwani, "Algorithms for VLSI Physical Design Automation", 3rd edition, Springer International Edition, 2005.

REFERENCES:

1) Hill & Peterson, "Computer Aided Logical Design with Emphasis on VLSI", Wiley, 1993.

2) Wayne Wolf, "Modern VLSI Design: Systems on silicon", Pearson Education Asia, 2nd Edition,1998.

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CMOS DIGITAL IC DESIGN

UNIT I

MOS Transistor: MOS Structure, MOS System under external bias, Structure and operation of MOSFET, Threshold voltage, MOSFET operation: A qualitative view.

UNIT II

MOSFET Current-voltage characteristics: Gradual channel approximation, Channel length modulation, Substrate bias effect, Constant field scaling, constant voltage scaling, short channel effects, Narrow channel effects.

UNIT III

MOSFET Models and Capacitance: Oxide-related capacitance, Junction capacitance. Level1, Level2, Level 3 modeling equations.

UNIT IV

CMOS Inverter: Circuit operation, calculation of VIL, VIH, Vth. Design of CMOS inverters, Supply scaling in CMOS inverter, Power and area considerations.

CMOS Inverter switching characteristics: Delay-time definition, calculation of delay times, Inverter design with delay constraints.

UNIT V

Estimation of Interconnects parasitic: Interconnect capacitance estimation, Interconnect resistance estimation. Calculation of Interconnect delay: RC delay Models, The Elmore delay, switching power dissipation of CMOS inverter, Power delay product.

UNIT VI

Sequential MOS logic circuits: Behavior of Bi-stable elements, SR Latch circuit, Clocked SR latch, Clocked JK Latch, Master-Slave flip-flop, CMOS D-Latch and Edge-Triggered Flip-Flop.

TEXT BOOKS:

1. Sung-Mo Kang & Yusuf Leblebici, “CMOS Digital Integrated Circuits - Analysis & Design”, , Second Ed., 1999.
2. Jan M Rabaey, “Digital Integrated Circuits - A Design Perspective”, Prentice Hall, 1997.

REFERENCES:

1. Eugene D Fabricus, “Introduction to VLSI Design,”McGraw Hill International Edition.1990.
2. R. J. Baker, H. W. Li, and D. E. Boyce, “CMOS circuit design, layout, and simulation”. New York: IEEE Press, 1998.
3. Ken Martin, “Digital Integrated Circuit Design”, Oxford University Press, 2000.

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I Year M.Tech (EMVL) – II Sem T C

LOW POWER VLSI DESIGN

(ELECTIVE - I)

UNIT I

LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

UNIT II

MOS/BiCMOS PROCESSES: Bi-CMOS processes, Integration considerations.

UNIT III

Bi-CMOS Isolation considerations.

LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes, SOI CMOS.

UNIT IV

DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models,

UNIT V

Sub-half micron MOS devices: Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT VI

CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.

TEXT BOOKS:

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl (3 Authors)-Pearson Education Asia 1st Indian reprint,2002.
2. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, KAP, 2002.

REFERENCES:

1. Digital Integrated circuits, J.Rabaey PH. N.J 1996
2. CMOS Digital ICs Sung-mo Kang and yusuf leblebici 3rd edition TMH 2003 .
3. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

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HARDWARE SOFTWARE CO- DESIGN
(Elective-I)

UNIT I

CO- DESIGN ISSUES: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

UNIT II

HARDWARE/SOFTWARE CO- SYNTHESIS ALGORITHMS: Introduction, preliminaries, Architectural model hardware – software partitioning, distributed system co-synthesis.

UNIT III

PROTOTYPING AND EMULATION: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping, system communication infrastructure

UNIT IV

TARGET ARCHITECTURES: Architecture Specialization techniques, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), and Mixed Systems.

UNIT V

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT VI

DESIGN SPECIFICATION AND VERIFICATION: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, and interface verification

TEXT BOOKS:

1. Jorgen Staunstrup, Wayne Wolf, “Hardware / software co- design Principles and Practice”, Springer, 2009.
2. Kluwer, “Hardware / software co- design Principles and Practice”, academic publishers,2002

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DEVICE MODELLING
(ELECTIVE-I)

UNIT I:

Introduction to Semiconductor Physics: Review of Quantum Mechanics, Boltzman transport equation, continuity equation, Poisson equation

UNIT_II

Integrated Passive Devices: Types and Structures of resistors and capacitors in monolithic technology, dependence of model parameters on structures

Integrated Diodes: Junction and Schottky diodes in monolithic technologies – static and dynamic behavior –small and large signal models – SPICE models

UNIT-III

Integrated Bipolar Transistor: Types and structures in monolithic technologies – Basic model (Eber-Moll) –Gunmel - Poon model- dynamic model, parasitic effects – SPICE model –parameter extraction

UNIT-IV

Integrated MOS Transistor: nMOS and pMOS transistor – threshold voltage – threshold voltage equations –MOS device equations – Basic DC equations second order effects – MOS models – small signal AC characteristics – MOS FET SPICE model level 1, 2, 3 and 4

UNIT V:

VLSI Fabrication Techniques-I: An overview of wafer fabrication, wafer processing – oxidation – patterning –diffusion – ion implantation – deposition

UNIT VI:

VLSI Fabrication Techniques-II: Silicon gate nMOS process – CMOS processes – n-well- p-welltwin tub- Silicon on insulator – CMOS process enhancements – interconnects circuit elements

TEXT BOOKS:

1. Introduction to Semiconductor Materials and Devices – Tyagi M. S, 2008, John Wiley Student Edition.
2. Solid state circuits – Ben G. Streetman, Prentice Hall, 1997

REFERENCES:

1. Physics of Semiconductor Devices – Sze S. M, 2nd edition, Mcgraw hill, New York, 1981
1. Introduction to Device Modeling and Circuit Simulation – Tor A. Fijedly, Wiley-Interscience, 1997

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ADVANCED DSP & APPLICATIONS
(Elective –II)

UNIT I

LTI DISCRETE-TIME SYSTEMS IN THE TRANSFORM DOMAIN: Types of Linear-Phase transfer functions, Complementary Transfer Functions, Inverse Systems, System identification, Digital Two-Pairs.

UNIT II

DIGITAL FILTER STRUCTURE AND DESIGN: All pass filters, Tunable IIR Digital filter, IIR & FIR tapped Cascaded Lattice Structures, Parallel All pass realization of IIR Transfer Functions, Digital Sine-Cosine generator.

UNIT III

Computational Complexity of Digital filter Structures, Design of IIR filter using pade‟ approximation, Least square design methods, Design of computationally efficient FIR filters.

UNIT IV

DSP ALGORITHMS: FFT, Sliding Discrete Fourier transform, DFT Computation Over a narrow Frequency Band, Split Radix FFT, Linear filtering approach to Computation of DFT using Chirp ZTransform.

UNIT V

ADAPTIVE FILTERS: FIR adaptive filters - Widrow-Hoff LMS adaptive algorithms and implementation, Adaptive channel equalization - adaptive echo cancellation - Adaptive noise cancellation - Adaptive recursive (IIR) filters – RLS algorithms and its applications( ), Introduction to Kalamaan filter.

UNIT VI

APPLICATIONS OF DIGITAL SIGNAL PROCESSING: Dual Tone Multi-frequency Signal Detection, Spectral Analysis using DFT, Short term discrete Fourier Transform, Musical Sound Processing, Digital FM stereo generation.

TEXT BOOKS:

1) Digital Signal Processing by Sanjit K Mitra, Tata MCgraw Hill Publications, 1st edition, 1999.
2) Digital Signal Processing Principles, Algorithms,Applications By J G Proakis, D G.Manolokis, PHI, 3rd edition, 2003.
3) Adaptive filter theory by Simon Haykin, Pearson education, 4th edition, 2003.

REFERENCES:

1) Discrete time signal processing by A.V.Oppenhiem, R.W. Schafer, Pearson education Asia, 2nd edition, 1996.
2) Statistical and adaptive signal processing by Dimitris G Manolakis & Vinay K.Ingle, McGraw Hill, 2000.

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NETWORK SECURITY & CRYPTOGRAPHY

(ELECTIVE - II)

UNIT I

INTRODUCTION: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internet work security. CLASSICAL TECHNIQUES: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT II

MODERN TECHNIQUES: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

ALGORITHMS: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.

UNIT III

CONVENTIONAL ENCRYPTION: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

PUBLIC KEY CRYPTOGRAPHY: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT IV

NUMBER THEORY: Prime and Relatively prime numbers, Modular arithmetic, Fermat‟s and Euler‟s theorems, Testing for primality, Euclids Algorithm, the Chinese remainder theorem, Discrete logarithms.

MESSAGE AUTHENTICATION AND HASH FUNCTIONS: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT V

HASH AND MAC ALGORITHMS: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC. DIGITAL SIGNATURES AND AUTHENTICATION PROTOCOLS: Digital signatures, Authentication Protocols, Digital signature standards.

UNIT VI

AUTHENTICATION APPLICATIONS: Kerberos, X.509 directory Authentication service.

ELECTRONIC MAIL SECURITY: Pretty Good Privacy, S/MIME.

TEXT BOOKS:

1. Cryptography and Network Security: Principles and Practice - William Stallings, Pearson Education., 2000.
2. Network Security by Bernard Menezes, Cenage learning, 2010.

REFERENCE:

1. Introduction to cryptography & Network Security by D.A.Forouzen, Tata McGraw Hill, 2008

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MICRO ELECTROMECHANICAL SYSTEMS
(ELECTIVE-II)

UNIT –I

Introduction, basic structures of MEM devices – (Canti-Levers, Fixed Beams diaphragms). Broad Response of Micro electromechanical systems (MEMS) to Mechanical (Force, pressure etc.) Thermal, Electrical, optical and magnetic stimuli, compatibility of MEMS from the point of power dissipation, leakage etc.

UNIT –II

Review of mechanical concepts like stress, strain, bending moment, deflection curve. Differential equations describing the deflection under concentrated force, distributed force, distributed force, deflection curves for canti-levers- fixed beam.

UNIT –III

Electrostatic excitation – columbic force between the fixed and moving electrodes.
Deflection with voltage in C.L, Deflection Vs Voltage curve, critical fringe field – field calculations using Laplace equation. Discussion on the approximate solutions – transient response of the MEMS.

UNIT – IV

Two terminal MEMS - capacitance Vs voltage Curve – variable capacitor. Applications of variable capacitors.Two terminal MEM structures.

UNIT-V

Three terminal MEM structures – controlled variable capacitors – MEM as a switch and possible applications.

UNIT – VI

MEM circuits & structures for simple GATES- AND, OR, NAND, NOR, Exclusive OR<simple MEM configurations for flip-flops triggering applications to counters, converters. Applications for analog circuits like frequency converters, wave shaping. RF Switches for modulation. MEM Transducers for pressure, force temperature. Optical MEMS.

TEXT BOOKS:

1. MEMS Theory, Design and Technology - GABRIEL. M.Review, R.F.,2003, John wiley & Sons. .
2. Strength of Materials –Thimo Shenko, 2000, CBS publishers & Distributors.
3. MEMS and NEMS, Systems Devices; and Structures - Servey E.Lyshevski, 2002, CRC Press.

REFERENCES:

1. Sensor Technology and Devices - Ristic L. (Ed) , 1994, Artech House, London.